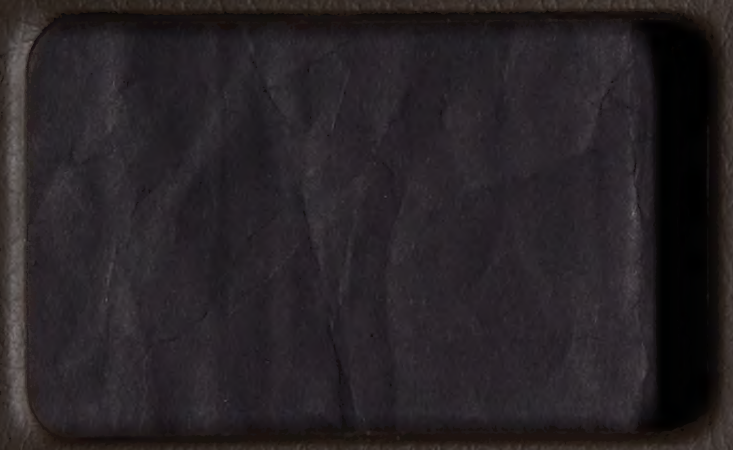

SOLARTRON
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TECHNICAL DATA

D. Lenby.

LM 1490
DIGITAL
VOLTMETER

Part No. 14900288	Date of Issue: June 1971

THE SOLARTRON ELECTRONIC GROUP LTD
Farnborough · Hampshire · England · Telephone 44433
Cables: Solartron Farnborough, Hants · Telex: 85245 Solartron Fnbro

©

DETAILS OF THE

EX1493 ZENER REFERENCE UNIT

AND

EX1494 MULTIMETER UNIT

ARE GIVEN AT THE BACK OF THIS MANUAL

SOLARTRON
Schlumberger

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LM 1490

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CIRCUIT DIAGRAMS AND COMPONENT PARTS LISTS

Accessories
Earthy Section Assembly
Counter Mother Board
Floating Box Assembly
Power Supply P.C.B. (Position 1)
Auto-Cal Logic P.C.B. (Position 2)
10^5 Reversible Decade P.C.B. (Position 3)
Reversible Decade Counter (Positions 4, 6, 8, 9 and 11).
Auto-Range P.C.B. (Position 5)
Timer Counter P.C.B. (Position 7)
Control Logic P.C.B. (Position 10)
Relay Drive P.C.B. (Position 12)
Decimal Point Drive System and Front Panel Switching (Position 13)
Positive Logic Fan Out Unit EX1488 (Positions 14 and 15)
Flux Oscillator (Position 16)
Input Switching (Position 17)
Floating Power Supply (Position 18)
Buffer Amplifier P.C.B. (Position 20)
Input Amplifier P.C.B. (Position 21)
Quantised Charge Generator (Position 22)
Clock and Positive Auto-Cal Amplifier (Position 22)
V to f Converter (Position 23)
EX1491 D.C. Unit
EX1492 External Calibration Unit

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SECTION 1 GENERAL

INTRODUCTION

The LM1490 Digital Voltmeter when used in conjunction with one of its associated sub-units is a fully programmable, high precision instrument with maximum resolution of 1 part in 250 000 and 100n V sensitivity. Fully automatic calibration at regular intervals (approximately once per minute) ensures high accuracy at all times. A comprehensive choice of operating speeds and interference rejection facilities, including mains synchronised integration, is provided, and in auto-checkout, data logging and process monitoring applications, LM 1490 is fully programmable by remote command. The AUTO-RANGE facility enables measurements to be made with minimum operator effort and to the best accuracy.

SPECIFICATION

	(421*)	RANGE	SENSITIVITY	INPUT RESISTANCE
D.C. RANGE ON 2 SEC INTEGRATION TIME	000	20mV	0.1μV	>100MΩ
D.C. RANGES ON 200mS INTEGRATION TIME	001	200mV	1μV	>100MΩ
	010	2V	10μV	>10GΩ
	011	20V	100μV	>10GΩ
	100	200V	1mV	10MΩ
	101	1000V	10mV	10MΩ

* BCD range identification

All ranges are capable of 10% over-ranging.

INTEGRATION PERIOD	SETTLING TIME TO 0.01% FROM ANY READING NOT IN OVERLOAD	SETTLING TIME TO 0.01% FROM 1000% OVERLOAD	TOTAL CONVERSION TIME TO 0.01%	RESOLUTION	SENSITIVITY
2mS	3mS	10mS	5mS	2000	10μV
2mS x 2	3mS	10mS	35mS	2000	10μV
20mS	3mS	10mS	23mS	20000	1μV
20mS x 2	3mS	10mS	73mS	20000	1μV
200mS	3mS	10mS	203mS	200000	0.1μV
200mS x 2	3mS	10mS	433mS	200000	0.1μV
2S	3mS	10mS	2.003S	200000	0.1μV
2S x 2	3mS	10mS	4.033S	200000	0.1μV

A x 10 TIME MULTIPLIER will increase all the above times, with the exception of the 2S time, by a factor of 10. This button does not increase the resolution. It is essential that this button is used on the 20mV Range to minimise noise.

ACCURACY

Using Internal Standard

For 200000 Resolution:- ±0.004% of reading ±0.001% F.S.D. ±1μV

For 20000 Resolution:- ±0.005% of F.S.D. ±1μV

For 2000 Resolution:- ±0.05% of F.S.D. ±10μV.

Using External Reference and EX1492 Sub-Unit

±0.003% of reading ±0.001% of F.S.D. ±1μV

STABILITY

Stability of internal standard cells:- 0.003% per six months 20mV, 200mV, 2V and 20V Ranges <±0.002% per six months. Typical ±0.001% for 90 days. 200V and 1000V Ranges:- <±0.004% per six months.

TEMPERATURE COEFFICIENT OF CALIBRATION

Allow at least one hour for internal thermal stabilisation. Wherever possible the voltmeter should be left switched on.

Range	Auto-cal Against Internal Standard Cells	Auto-cal Against External Reference
2V	5 p.p.m/°C	1 p.p.m /°C
20mV, 200mV 20V	7 p.p.m/°C	3 p.p.m/°C
200V, 1000V	10 p.p.m/°C	6 p.p.m/°C

TEMPERATURE COEFFICIENT OF ZERO

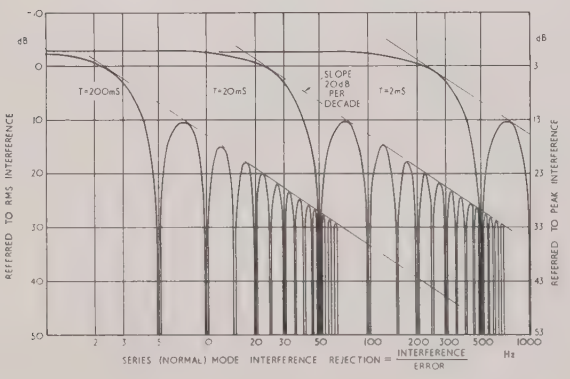
±0.0002% of F.S.D./°C ±0.3μV/°C.

SERIES MODE REJECTION

FREQUENCY	INTEGRATION TIME	REJECTION
50Hz ±1Hz	20mS	30dB
50Hz ±10Hz	20mS x 2	40dB
50Hz ±1Hz	20mS x 2	60dB
50Hz ±1Hz	200mS	50dB
50Hz ±1Hz	2S	70dB

The above rejection figures using LINE SYNC (x 2) apply with up to 3% even harmonic distortion.

Maximum permissible peak series mode signal, 25% of signal at full scale reading.



FILTER

Single 100mS lag.

30dB attenuation at 50Hz increasing at 6dB/octave (20dB/decade). Settling time to 0.01% is 4 sec. (1 sec nominal plus 3 sec. because of dielectric absorption of the filter capacitor).

COMMON MODE REJECTION

With Guard strapped to LO and 1kΩ unbalance in the LO lead.

D.C. : 140dB

50Hz : 70dB + Series Mode Rejection

Maximum Guard to Earth Voltage 500V peak

Maximum Guard to LO Voltage 100V peak

Maximum Guard to Earth Step Voltage 200V.

OPERATING MODES

1) AUTO (Continuous tracking of input voltage)

2) MANUAL:-
   a) Front Panel Push Button
   b) Contact Closure
   c) Pulse

3) RANGE CHANGE MODES
   a) Manual
   b) Auto (Limited to 200V Range)
   c) Remote Control

REAR PANEL FACILITIES

Auto-Cal Command: Internal/Remote; switch.

Print out: Without Fan Out boards, none.

Programmable Fan Out Boards, [+5V and +12V logic] available.

MAINS INPUT

117/234V ±15% 50-60Hz

Power Consumption 50VA.

ENVIRONMENTAL SPECIFICATIONS

Working Temperature Range to Full Specification 10°C–35°C.

Working Temperature Range to Limited Specification 0°C–50°C (Due to Standard Cells).

Storage Temperature Range with Standard Cells -10°C to +55°C.

Storage Temperature Range without Standard Cells -25°C to +75°C

Maximum Humidity Working 60%.

DIMENSIONS;			
	Height	131mm	[5.19in]
	Width	447mm	[17.6in]
	Depth	565mm	[22.25in]
	Weight	20kg	[45lbs]

SECTION 2
OPERATING INSTRUCTIONS

Display : *Numerals and polarity displayed by cold cathode tubes. Decimal points displayed by end viewed neons.*

2000—— Full scale length with 2mS INTEGRATION TIME.

20000– Full scale length with 20mS INTEGRATION TIME.

200000 Full scale length with 200mS INTEGRATION TIME.

x10 and x2 (LINE SYNC) do not alter the scale length.

Indicator for displaying units (V or mV) and ✱. ✱ is displayed when reading exceeds full scale by 10% and during AUTO-CAL.

Range Selector: *Ten position switch selects:–*

a) 20mV, 200mV, 2V, 20V, 200V or 1000V range, with automatic decimal point and units (mV or V) setting.

b) nV OFFSET: for zero setting on 20mV and 200mV ranges when short circuiting input leads is undesirable.

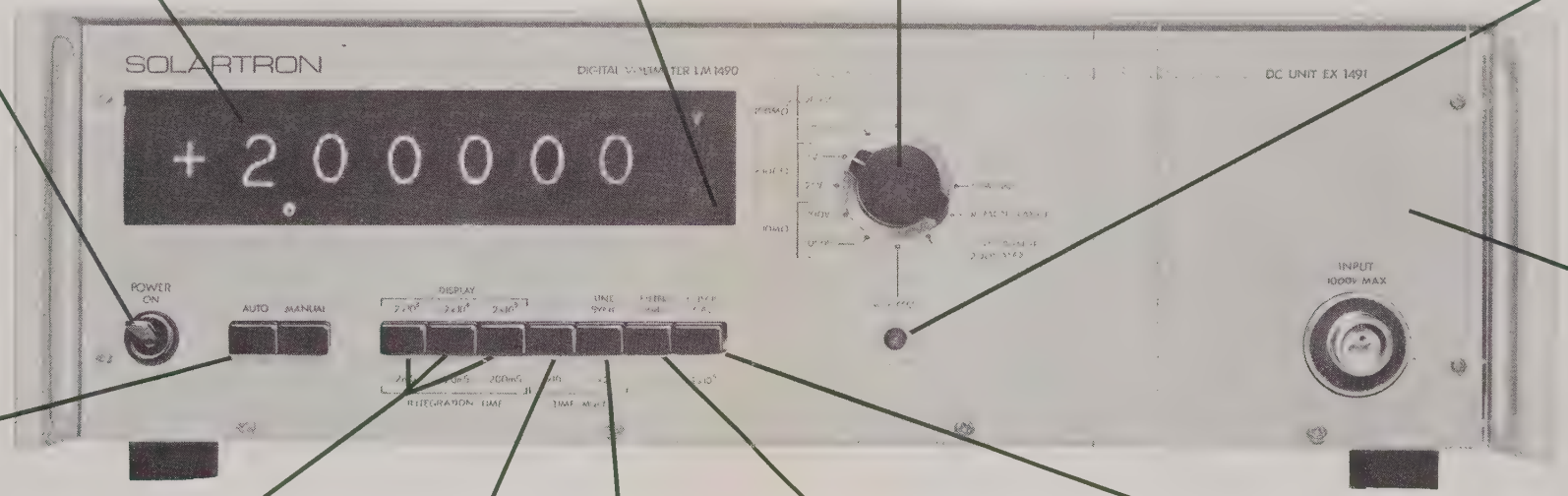
c) AUTO RANGE 200V MAXimum: for automatic selection of optimum range from 20mV to 200V ranges.

d) REMOTE RANGE: (200V Maximum) for remote control of ranges by commands to rear socket.

e) SUB-UNIT: for control by appropriate sub-unit.

nV OFFSET: *A ten turn potentiometer for zero setting on the 20mV and 200mV ranges.*

POWER ON: *Toggle switch for applying mains power to the instrument.*



AUTO MANUAL: *Two push buttons commanding repetitive or single shot sample. Initial depression of the MANUAL button releases the AUTO button.*

Each subsequent depression of the MANUAL button commands display of a new measurement.

Sub-unit, on which the INPUT Connector is mounted. (See SUB-UNITS).

INTEGRATION TIME: *Three push buttons which control the scale length and sample rate.*

TIME	SAMPLE RATE	SCALE LENGTH
2mS	500/sec	2000
20mS	50/sec	20000
200mS	5/sec	200000

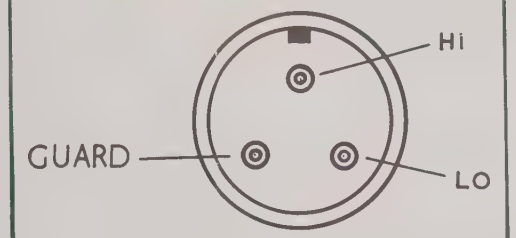
x10 TIME MULTiplier: *Push button switch increases INTEGRATION TIME by a factor of ten, giving improved rejection of low frequency interference.*

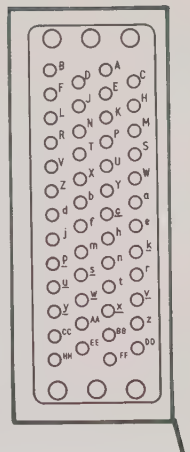
LINE SYNChronised: *Push button switch selects mains synchronised integration which gives additional rejection of mains derived interference by controlling integration to compensate for variations of supply frequency.*

FILTER 30dB: *Push button switch selects a single section low pass filter, which gives an additional 30dB series mode rejection at 50Hz increasing at 6dB/Octave. Provides rejection of wide band noise.*

CHECK CALibration: *Push button switch when momentarily pressed initiates an AUTO-CAL run. ✱ is displayed for the duration of the AUTO-CAL run. If the switch is held in for longer than the duration of AUTO-CAL, the display will show the normalised reference voltage i.e., 2000, 20000 or 200000 ±2 bits, for INTEGRATION TIMES (basic) of 2mS, 20mS or 200ms respectively. The decimal point remains in the position determined by the range switch.*

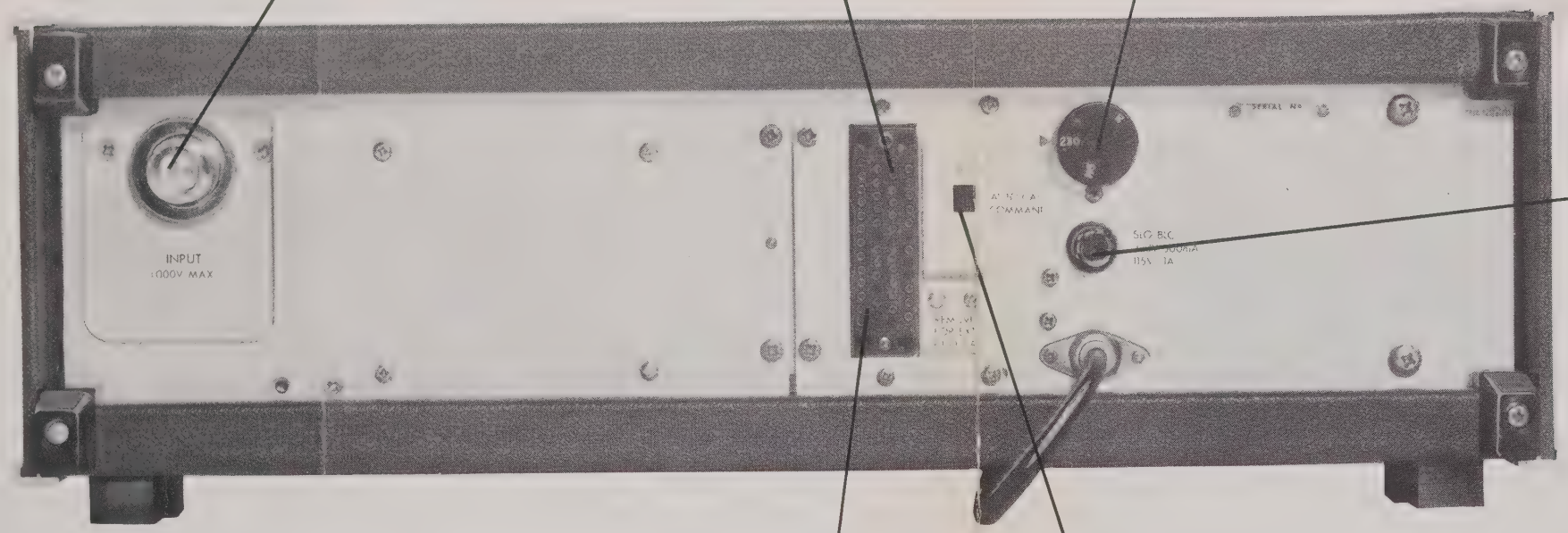
INPUT connector: *Three pole connector wired in parallel with front connector.*





Mains Selector Plug selects 115V or 230V (Nominal) mains operation. To change from 230 to 115, or vice versa, pull out and turn until required voltage is opposite.▸. Push in.

FUSE HOLDER
Normally fitted with 500mA SLO-BLO fuse for 230V operation. This must be changed to 1A SLO-BLO for 115V operation.



Information Connector (SKA): *A 50 way socket carrying information and to which remote commands are applied.*
Facilities provided by the connector are:-

- *(a) Range Information (421 BCD)*
- *(b) Remote AUTO-CAL command*
- *(c) Clock frequency*
- *(d) Initiation of a single measurement (Digitise Command) by:-*
  - *(i) Contact Closure*
  - *(ii) Pulse*
  - *Available only with Fan Out Unit*
- *(e) Remote Range command (421 BCD)*
- *(f) Remote command of INTEGRATION TIME.*
- *(g) Remote FILTER command.*
- *(h) With Fan Out Unit, BCD display information Polarity information. See FAN OUT UNIT.*

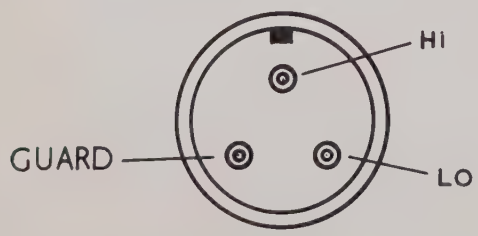
AUTO-CAL COMMAND: *Slide switch giving option of INTernal or EXTernal command of AUTO-CAL. Normally held in INTernal position by blanking plate. With switch at INT. external commands can be applied in addition to those generated internally. In EXT position AUTO-CAL commanded by remote control and CHECK CAL button.*

D.C. UNIT EX1491

EX1491 is the sub-unit supplied as a standard item with LM1490. Contained inside are unsaturated Weston cells against which the LM1490 is regularly calibrated.

CONNECTORS

INPUT 1000V MAXimum: *Three pole connector, containing Hi, Lo and GUARD, to which the input signal is applied via a screened cable.*



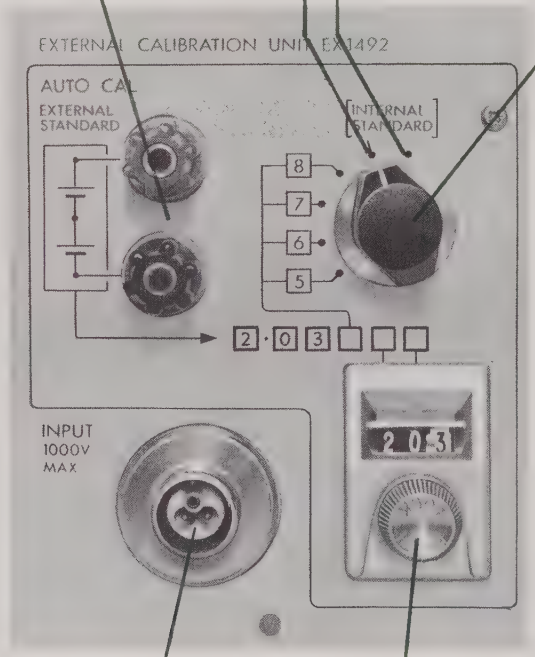
EXTERNAL CALIBRATION UNIT EX1492

Sub-unit EX1492 provides a choice of calibration standards. Either the internal unsaturated reference cells or the users own reference source may be used. The external reference range is 2.03500V to 2.03900V so that the external reference may be obtained from series connected, saturated or unsaturated, standard cells.

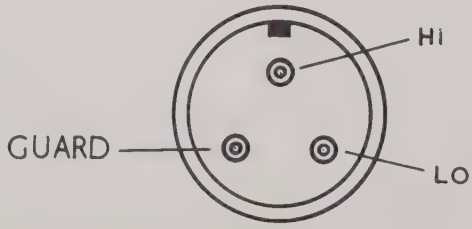
CONTROLS AND CONNECTORS

Selector: *Six position rotary switch selects:-*
i) INTERNAL STANDARD: *for calibration of LM1490 against the internal standard cells.*
ii) 8, 7, 6 or 5mV: *selected to equal the fourth significant figure of the sum of the external reference sources.*
iii) *a position which disconnects the internal cells, for storage purposes.*

EXTERNAL STANDARD : *Two 4mm terminals to which the external calibration reference source is connected.*



INPUT 1000V MAXimum: *Three pole connector, containing Hi, Lo and GUARD, to which the input signal is applied via a screened cable.*



Calibrated Dial: *adjusted to display the fifth and sixth significant figures, of the sum of the external reference sources. Adjustment is made by pulling the spindle knob, turning until the correct value is displayed and pushing the spindle knob to lock the result.*

FAN OUT UNIT EX1488

The EX1488 is a positive logic Fan Out Unit, comprising two printed circuit cards, which enables 8421 BCD display information to be presented at the LM1490 rear socket. The Units are normally supplied to drive systems which use 0V and +5V logic levels but, by changing two wire links (one per board) the levels can be changed to 0V and +12V.

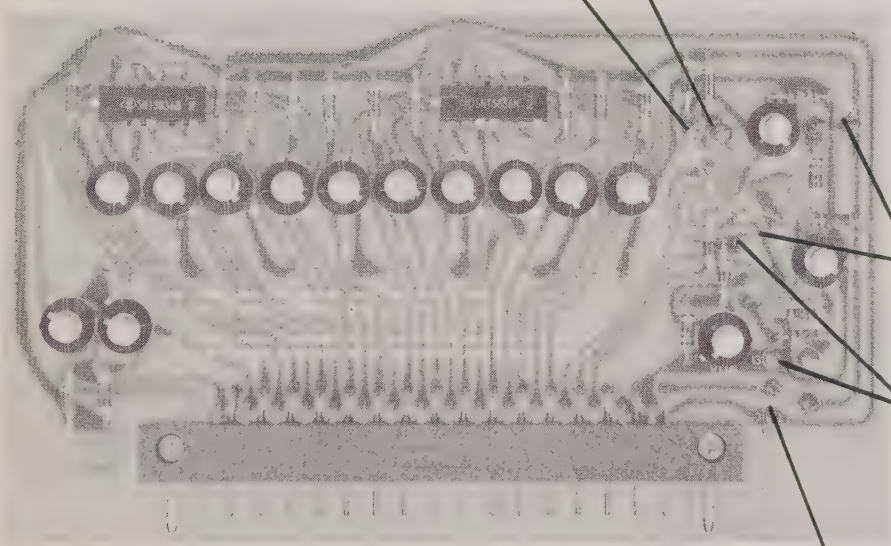
FAN OUT POSITION 14

Link 4 to 5 for positive going PRINT COMMAND level at pin v on the rear socket.

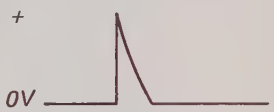
Normally supplied in this configuration

OR

Link 4 to 6 for negative going PRINT COMMAND Level at pin v on the rear socket.



Link 8 to 9 and 10 to 11 for positive going PRINT COMMAND pulse at pin u on rear socket.



Normally supplied in this configuration.

OR

Link 7 to 8 and 12 to 13 for negative going PRINT COMMAND pulse at pin u on rear socket.

Link 1 to 2 for 0V and +12V logic levels.
Link 1 to 3 for 0V and +5V logic levels.
Normally supplied with 1 to 3 linked.

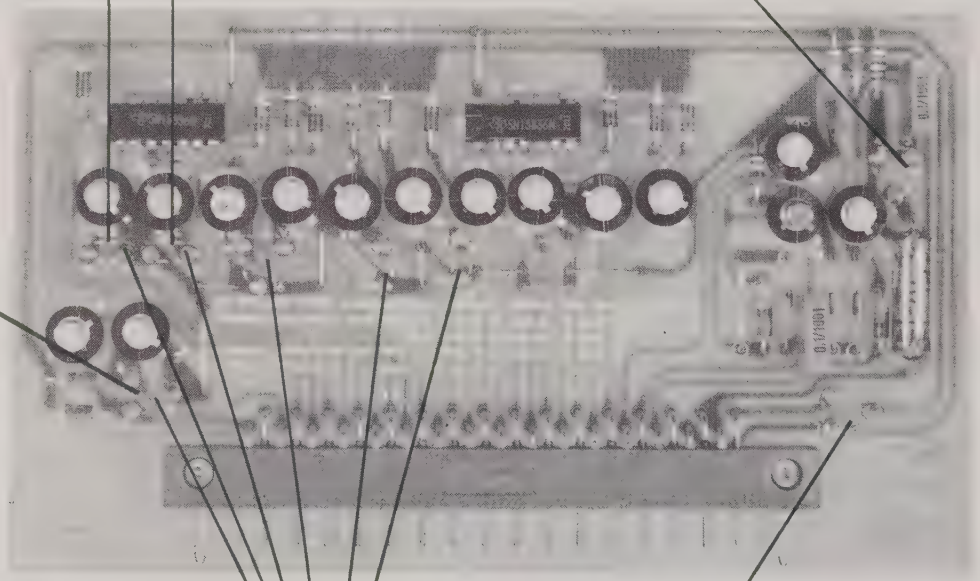
FAN OUT POSITION 15

Link 7, 8 and 9 together, 10 to 11 and 12 to 13, to give the output:-

Pin D (8_0)	Pin C (4_0)	Pin B (2_0)	Pin A (1_0)
1	1	0	0

i.e. decimal 12 from the least significant (10^0) decade. May be used to call up SPACE when LM1490 is used in data logging applications.

Link 4, 5 and 6 together, to provide noise immunity when using contact closure (between pins s and HH) to initiate a measurement (sample).



Link 7, 8, and 9 together, 10 to 11; 12 to 13; 14, 15 and 16 together; 17 to 18 and 19 to 20 to give the output:-

Pin J (8_1)	Pin H (4_1)	Pin F (2_1)	Pin E (1_1)
1	1	0	0

Pin D (8_0)	Pin C (4_0)	Pin B (2_0)	Pin A (1_0)
1	1	0	0

(i.e. decimal 12) from the least significant (10^0) and (10^1) decades. May be used to call up SPACE(S) and/or special characters, for data logging applications.

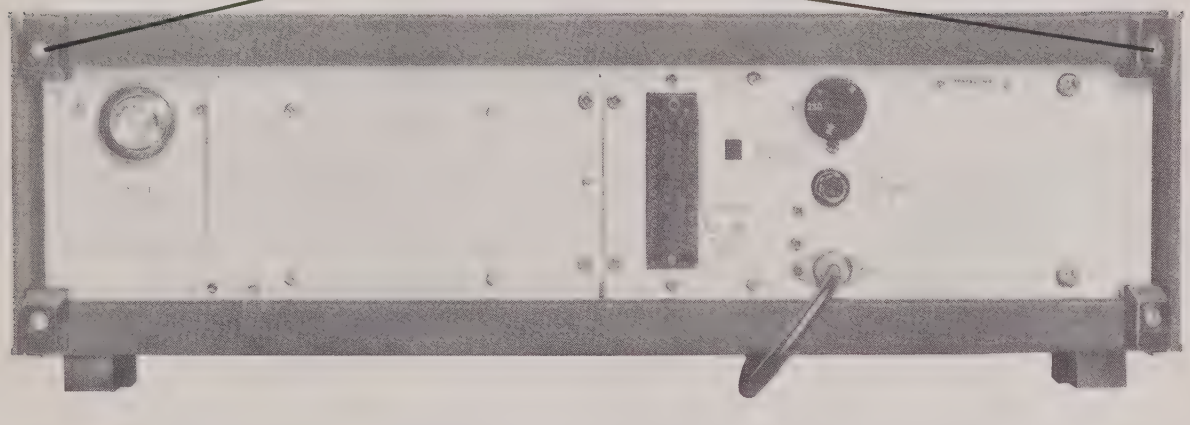
Link 1 to 2 for 0V and +12V logic levels. Link 1 to 3 for 0V and +5V logic levels. Normally supplied with 1 to 3 linked.

Outputs
Common emitter transistor stages with 1.5kΩ load to nominal +12V or +5V supply, capable of sinking a further 10mA.

Pulse Sample
Pulse amplitude: between 3V and 8V
Duration: >10μS
Input Impedance: >10kΩ

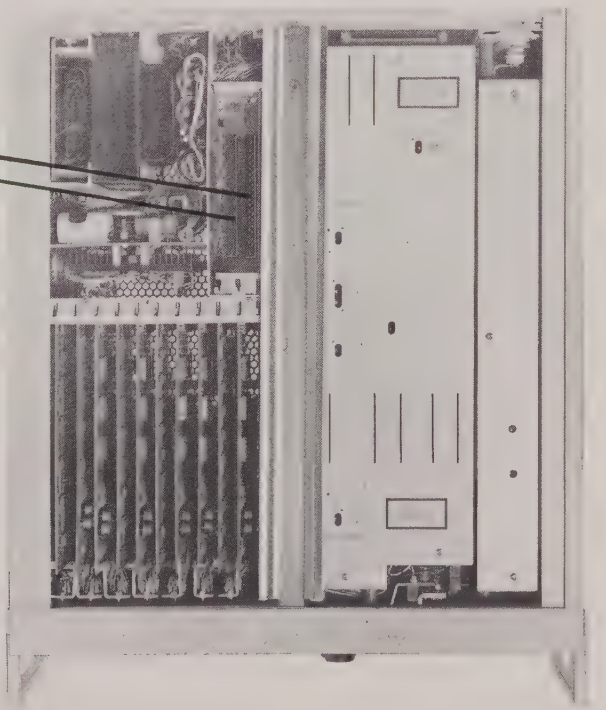
Installing Fan-out Units

1. Remove the two screws which secure the plastic feet and withdraw the instrument top cover.



2. Slacken the two screws which secure the board clamp and remove the clamp.

3. Insert the two Fan-Out printed circuit cards and press home. Position 14, Position 15



4. Replace top cover and plastic feet and secure.

PIN	SERVICE	REMARKS	PIN	SERVICE	REMARKS
A	1_0	10^0 Decade Display Information	d	PRINT +	With Fan-Out only
B	2_0	when INTEGRATION TIME is	e	PRINT -	With Fan-Out only
		200mS.	f	(1) Range	
C	4_0	Can be programmed to decimal	h	(2) Indication	See Output Information
D	8_0	12. See Fan-Out Unit.	j	(4)	
E	1_1	10^1 Decade Display Information	k		Not used
F	2_1	when INTEGRATION TIME is	m	(1)	
H	4_1	200mS or 20mS. Can be	n	(2) Range	See Remote Commands
J	8_1	programmed to decimal 12.	p	(4) Commands	
		See Fan-Out Unit			
K	1_2				
L	2_2	10^2 Decade Display	r		Not used
M	4_2	Information	s	Contact Sample	With Fan-Out only
N	8_2	With Fan-Out only	t	Pulse Sample	See Remote Commands
P	1_3	10^3 Decade Display	u	PRINT	PULSE / See FAN OUT
R	2_3	Information	v	COMMAND	LEVEL / UNIT
S	4_3	With Fan-Out only	w		Not used
T	8_3		x	CLOCK	320kHz (50Hz) or 384kHz (60Hz)
U	1_4	10^4 Decade Display	y	AUTO-CAL COMMAND	See Remote Commands
V	2_4	Information	z	Filter	See Remote Commands
W	4_4	With Fan-Out only	AA	2mS	Integration times
X	8_4		BB	20mS	See Remote Commands
Y	1_5	10^5 Decade Display	CC	200mS	* SEE POSITION
Z	2_5	Information. With Fan-Out only	DD		
a		Not used	EE		Not used
b		Not used	FF		Not used
c		Not used	HH	0V	

REAR SOCKET SERVICES

Table 2.1

Remote Commands

Voltages are referred to 0V at pin HH, Hi = +2.5V to +5V Lo = 0V to +1V.

Range

Range	(4) Pin p	(2) Pin n	(1) Pin m
20mV	Lo	Lo	Lo
200mV	Lo	Lo	Hi
2V	Lo	Hi	Lo
20V	Lo	Hi	Hi
	Hi	Hi	Hi
200V	Hi	Lo	Lo

Table 2.2

Measurement (Sample. With Fan Out Unit only).

1) Pulse Sample

First press the MANUAL button to release the AUTO button.

Positive pulse at pin t of $>10\mu S$ duration and between 3V and 8V amplitude.

2) Contact Sample

First press the MANUAL button, to release the AUTO button. Contact closure between pin s and pin HH (0V). See 'Fan Out Unit' for details on noise (contact bounce etc.) immunity.

Output Information

All output information is presented at the rear socket. With the exception of Display information, voltages are:-

Hi = +2.6V to +5V

Lo = 0V to +0.4V

Display voltage levels are determined by links on the Fan Out Unit.

Range

Range	(4) Pin j	(2) Pin h	(1) Pin f
20mV	Lo	Lo	Lo
200mV	Lo	Lo	Hi
2V	Lo	Hi	Lo
20V	Lo	Hi	Hi
200V	Hi	Lo	Lo
1000V	Hi	Lo	Hi

Table 2.3

Clock: Clock frequency 320kHz (with 50Hz mains. 384kHz. with 60Hz mains) at pin x.

Display: Available with Fan Out unit only.

Integration time

Before integration time can be selected remotely, all INTEGRATION TIME push buttons must be in the 'out' position. This is achieved by depressing any "out" button half-way and releasing. The times can then be commanded by the link arrangement of table 2.4

INTEGRATION TIME	LINK
2 mS	AA to DD
20 mS	BB to DD
200 mS	CC to DD

Table 2.4

Filter

Ensure that the FILTER 30dB switch is 'out'

Link pin z to HH.

AUTO-CAL

With the AUTO-CAL COMMAND switch in the INTernal position AUTO-CAL commands can be applied in addition to those internally generated (and those from the CHECK CAL push button).

i) by contact closure between pin y and pin HH (0V) for not longer than 20mS

ii) by pulse application

at pin y from a source impedance of less than 100Ω (t=1μS to 20mS).

It is recommended that the frequency of AUTO-CAL commands be not less than the frequency of internally generated commands, except when the ambient temperature of the instrument is well within limits.

With the AUTO-CAL COMMAND switch in the EXTernal position, AUTO-CAL is selected only by the above commands and the CHECK CAL switch.

OPERATION

PRELIMINARY ADJUSTMENTS

Check that the mains selector plug is set to 115 for supply voltages between 100V and 130V, or to 230 for supply voltages between 200V and 260V. Also check that the fuse is either 1A SLO-BLO for 115V or 500mA SLO-BLO for 230V. Connect a suitable plug to the mains lead:-

BROWN	–	LINE
BLUE	–	NEUTRAL
GREEN/YELLOW	–	EARTH

CALIBRATION

Using D.C. UNIT EX 1491

With the input leads short circuited, 200mS INTEGRATION TIME, AUTO, and 20V Range selected, set the mains switch to POWER ON. The voltmeter starts automatic calibration immediately. A 'scrambled' reading is displayed until the end of the first calibration run when an off-set voltage is displayed. This off-set reading decreases after each calibration run until, after five minutes, zero is reached.

Calibration can be completed more rapidly by repeatedly pressing the CHECK-CAL button until, with the CHECK-CAL button out, zero is displayed, and with CHECK CAL button pressed for longer than the duration of AUTO-CAL (approx. 0.7 seconds) 200000 ±2 digits is displayed.

Using EXTERNAL CALIBRATION UNIT EX1492

When using the internal reference cells of EX1492 follow the procedure – 'Using D.C. UNIT EX1491.'

When calibrating against an external reference, before connecting it to the terminals of EX1492, the fourth, fifth and sixth significant figures of the reference value must be selected on the controls of EX1492.

With the input leads short circuited, 200mS INTEGRATION TIME, AUTO and 20V range selected, set the mains switch to POWER ON. The voltmeter starts automatic calibration immediately. A 'scrambled' reading is displayed until the end of the first calibration run when an off-set voltage is displayed. This off-set reading decreases after each calibration run until, after five minutes, zero is reached.

Select the 2V Range and connect the input leads to the external standard and momentarily press the CHECK CAL button to initiate an AUTO-CAL run. At the end of AUTO-CAL the display should be the same as the value of the reference. Slight adjustment of the calibration dial on EX1492, may be required to achieve this. Repeat the CHECK-CAL and dial adjustment alternately as required.

AUTO-CAL is performed on the 2V range. Full accuracy on other ranges will be achieved when a suitable warm-up time for the attenuator has been allowed.

VOLTAGE MEASUREMENT

Caution: The maximum inputs that can safely be applied to the instrument are:-

i) 200V on the 20mV, 200mV, 2V and 20V ranges.
ii) 1000V on the 200V and 1000V ranges.

1) Select an appropriate range. If the input voltage is unknown select the 1000V range. When the voltages to be measured are always less than 200V, readings can be obtained with minimum effort by selecting AUTO-RANGE.
2) Select AUTO or MANUAL operation as required. If MANUAL operation is selected in conjunction with AUTO-RANGE, the voltmeter will still find the correct range before displaying the new reading.
3) Select INTEGRATION TIME as required. (See Notes).
4) Connect the input lead to the unknown voltage source, red to signal Hi and black to signal Lo.
5) Read the voltage from the display, if necessary down ranging to obtain greater sensitivity. The indicated polarity is that of the red lead with respect to the black.

Notes

Although the instrument automatically calibrates itself every minute, momentary depression of the CHECK-CAL button (to initiate AUTO-CAL) prior to a measurement, regardless of the range selected, will ensure the greatest possible accuracy at the time of measurement.

Always use the longest integration time consistent with the sensitivity and resolution required. When increasing the integration time avoid increasing the sensitivity beyond a useful level.

For the best accuracy and good series mode rejection use the shortest scale length and the longest integration which this accommodates, e.g. 2mS INTEGRATION TIME x 10, and LINE SYNC. On all but the most sensitive range this will give an uncertainty of reading of ±1 digit.

When a reading occupies less than ten percent of the full scale, greater accuracy is achieved by down ranging, reducing INTEGRATION TIME by a factor of ten and selecting the x 10 TIME MULT facility. Thus the voltmeter will display the reading with the same sensitivity and in the same time as previously, but to a greater accuracy.

Example:

Range:	200mV
Integration time:	200mS
Reading:	020.000mV
Uncertainty:	±0.001% F.S.D.±1μV =±3.8μV.
New Range:	20mV
Integration time:	20mS + x10 TIME MULT. Total 200mS.
Reading:	20.000 – mV
Uncertainty:	±0.005% F.S.D. ±1μV=±2μV.

With AUTO-RANGE selected the previous operation is simplified so that only the integration time need be changed.

If the display shows an asterisk ✱ and the reading exceeds the nominal full scale by more than 10%, the instrument should be upranged. The display will show an ✱ when the reading is within the limits of the range in use, to indicate that AUTO-CAL is in progress.

If the displayed reading is unsteady, it may be stabilised by selecting a longer integration time, LINE SYNC or the 30dB FILTER, or any combination of these.

Where mains derived interference is a problem, the LINE SYNC facility provides excellent rejection, even when the mains supply frequency varies from the nominal 50Hz, without affecting resolution.

LOW LEVEL MEASUREMENTS

When using either the 200mV or 20mV range periodic adjustment of the nV OFFSET potentiometer may be necessary during the first sixty minutes after switch on, or until stabilisation of thermal effects occurs.

It is recommended that a minimum integration time of two seconds is selected when measurements are performed using the 20mV range. To achieve this, select 200mS x 10.

When using the two most sensitive ranges, a difference in zero may be observed. This is caused by the difference in the thermal characteristics of the two reeds used in selection of these ranges, and can be nulled by adjustment of the nV OFFSET control. On these ranges, neglect of the effects of input current, source resistance noise (Johnson Noise) and thermal e.m.f's can cause errors. For example, an input current of 10^{-10}A, through a source resistance of 10kΩ produces a potential difference of 1μV — i.e. 10 bits on the 20mV range or 1 bit on the 200mV range. For this reason low level measurement should be restricted to signals from source resistances of less than 1kΩ. Also, Johnson Noise $\doteq 1.3 \times 10^{-10} \sqrt{R\ \Delta f}$ volts r.m.s. where R = resistance and Δf = noise bandwidth. Thus, the noise contributed by a 10kΩ resistor at 100Hz bandwidth, is approximately 130nV r.m.s. The average value approaches zero only after a long period of time, thus the longer the measurement period the less effect noise will have on the measurement. Noise is reduced when the 30dB FILTER is selected.

Adequate precautions against the pick-up of interference must be taken when performing low level measurements, e.g. screen all signal leads.

Handling of the alligator clips will cause a rise in their temperature sufficient to produce an e.m.f. and the user should be aware of this.

Switching from a high voltage range (e.g. 200V) to the 20mV range, with the filter selected, will produce a decaying offset, caused by dielectric absorption of the filter capacitor. Although the use of a high grade component minimises this phenomenon it cannot be totally eliminated.

SECTION 3 TECHNICAL DESCRIPTION

PRINCIPLES OF OPERATION

Digital Voltmeter LM1490 has been developed from the basic system of a voltage to frequency (v to f) converter followed by a counter and display.

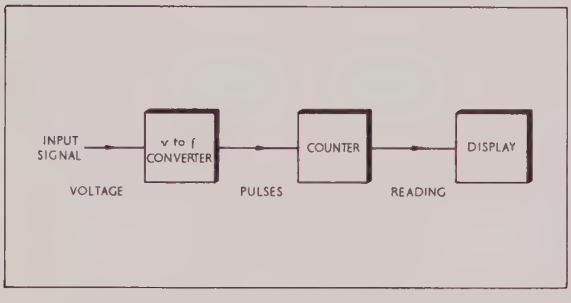


Fig. 3.1 Basic System

The v to f converter produces a pulse train at a rate linearly proportional to the value of the unknown voltage. The counter totals the number of pulses produced during a given time interval and the result is displayed. By suitable choice of parameters, principally count period and v to f ratio, the displayed total gives a direct reading of the unknown voltage.

This design concept confers a number of advantages upon the performance of the voltmeter, the most significant being:-

(1) **Integration:** The pulses generated are continuous and vary in frequency with the unknown voltage. The result of counting them over a fixed period of time is that the displayed total is the average value of the input over that time. Thus, if the time interval is made 20mS then the average of any 50Hz component is zero.

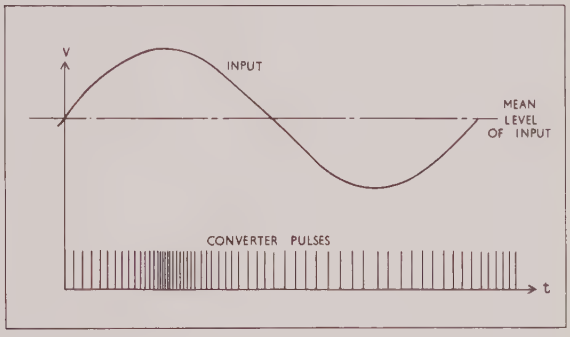


Fig. 3.2 Averaging Effect

(2) **Sensitivity:** By increasing the measurement period to 200mS, the number of pulses accumulated by the counter is increased by a factor of ten. Thus each pulse represents a smaller increment of the unknown voltage. It follows that the capacity of the counter will have to be increased to accommodate the increase in sensitivity. Hence an increase in scale length.

(3) **Isolation:** Communication between converter and counter is achieved exclusively by means of pulses. Their significance is their quantity rather than their shape or size. They can be coupled to the counter by means of small pulse transformers which have very low capcitance and very high leakage resistance. Hence, while the counter circuits can be connected to earth, the converter is very thoroughly isolated from earth.

However, there are two primary requirements of a voltmeter, (1) that it should have a high input impedance so that accuracy is maintained when measuring a voltage with a high source impedance and (2) that it is linear throughout its dynamic range.

The ways in which LM1490 satisfies these and other requirements are outlined below.

Linearity and Input Impedance

The high input impedance is achieved by a potentiometric system. i.e. the unknown is balanced against a known potential, the displayed reading being the known potential. The linearity is achieved by exploiting the high gain of an open loop d.c. amplifier.

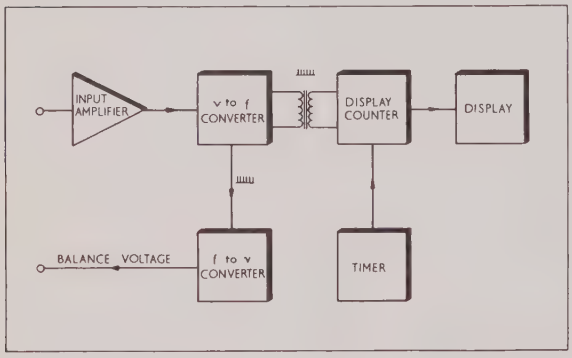


Fig. 3.3 Potentiometric Input System

The output from the v to f converter is applied to the f to v converter which produces a voltage proportional to frequency to oppose the unknown voltage. The amplifier detects the difference (error) between the balance voltage and the unknown voltage and causes the v to f converter to adjust its frequency until the balance voltage is equal to the unknown voltage, thus creating a balance condition. The frequency of pulses from the v to f converter is therefore directly proportional to the unknown voltage. The high gain of the input amplifier enables an error of considerably less than one microvolt to be detected. Thus the system is highly sensitive. Also, because at balance the error is extremely small, the input impedance is extremely high (of the order of $10^{10}\Omega$).

BI-POLAR OPERATION

To be capable of bi-polar operation an input change-over relay could be used. However, this has the disadvantage that a measurement must be made in order to detect wrong polarity. Also, the application of wrong polarity to the v to f converter may result in overload, and two or three new measurements may be necessary before the reading can be relied upon. Therefore a method of generating both positive and negative balance voltages is required. To effect this requirement, without a complex bi-polar f to v converter, an offset is inserted in the feedback line equal to half the maximum available output from a uni-polar f to v converter.

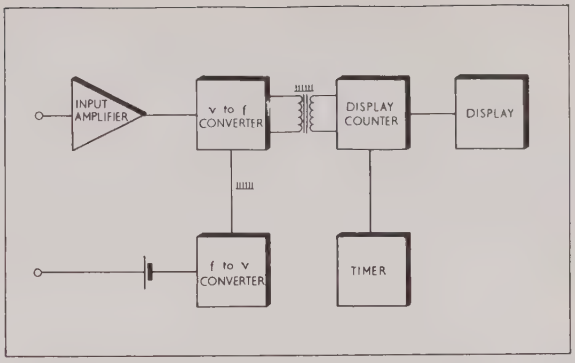


Fig. 3.4 Principle of Bi-polar Operations

Suppose the output of the f to v converter is in the range 0 to -2V and the offset is +V. For a full scale positive input of +V the f to v converter generates -2V which is offset by +V to give the correct balance voltage -V. Similarly for a full scale negative input of -V the f to v converter generates 0 which is offset by +V to give the correct balance voltage +V. Hence, with zero input the f to v converter must generate a potential equal in magnitude to the offset but of opposite polarity. To achieve this the v to f converter generates pulses at half its maximum frequency. For positive inputs the frequency must increase and for negative inputs the frequency must decrease.

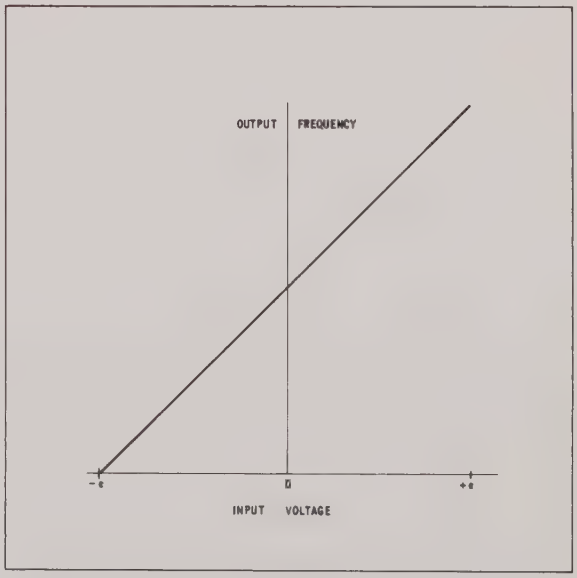


Fig. 3.5 v to f Converter Characteristic

Such a system requires a reversible counter, which counts backwards from negative full scale to zero and then forward from zero to positive full scale. The realisation of bi-polar operation is illustrated in Fig. 3.6.

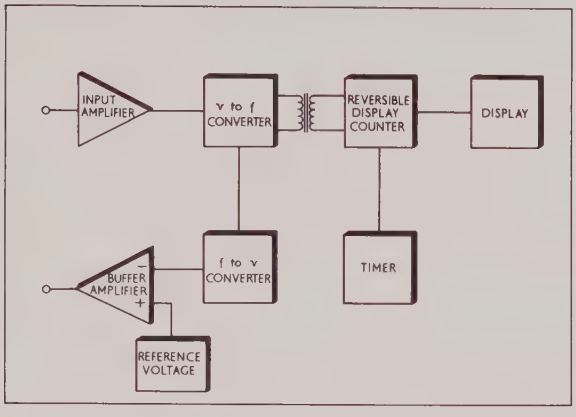


Fig. 3.6 Realisation of Bi-polar Operation

In the practical circuit, the offset is summed with the f to v converter output, at the differential inputs of a buffer amplifier. The use of an amplifier increases the balance voltage capability so that larger unknown voltages can be measured, without the use of an input attenuator which reduces the input impedance.

INCREASED SCALE LENGTH

The high sensitivity of the previous system enables the resolution to be improved by increasing the scale length. To achieve this it is necessary for the display counter to accumulate a greater number of pulses. This can be accomplished by increasing either the count period, or the frequency range of the v to f converter, or a combination of the two. However, while it is possible to have a v to f converter operating above 5MHz, the f to v converter is restricted in its frequency of operation by the finite switching speeds of transistors. Therefore a system which increases the v to f rate but retains the original f to v rate is required. The principles of such a system are illustrated in Fig. 3.7.

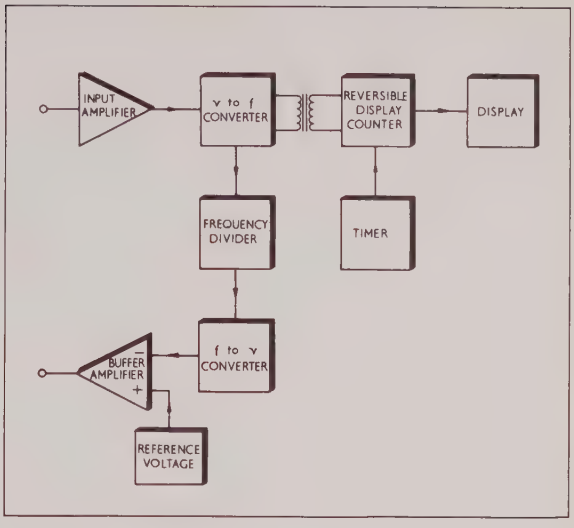


Fig. 3.7 Principle of Increased Scale Length

In order to generate the same magnitude balance voltage as before, the v to f converter must now operate at a higher frequency and thus generate a greater number of pulses during the count period. Increasing the count period increases the number of pulses counted still further.

In practice, a further modification to the arrangement of Fig. 3.7 is necessary, as analysis of the f to v converter reveals.

The f to v converter consists of a Quantised Charge Generator (QCG) followed by a filter. The QCG emits constant amounts of charge, in the form of pulses of defined width and amplitude, which are time averaged by the filter to provide the balance voltage. The width and amplitude of the pulses are defined by a crystal clock and a reference voltage respectively.

Their repetition rate is determined by the output from the frequency divider.

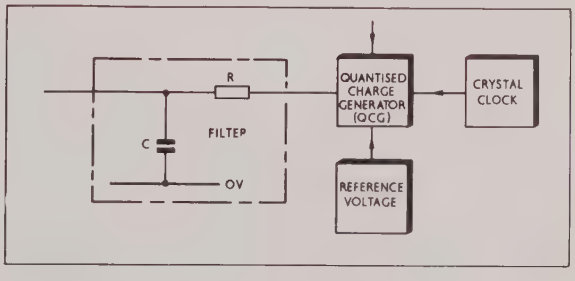


Fig. 3.8 The f to v converter

Unfortunately, as the rate at which QCG pulses are generated decreases, the filter smoothing becomes inefficient and therefore a more efficient method of smoothing which does not increase the filter time-constant is required. A practical solution is shown in Fig. 3.9.

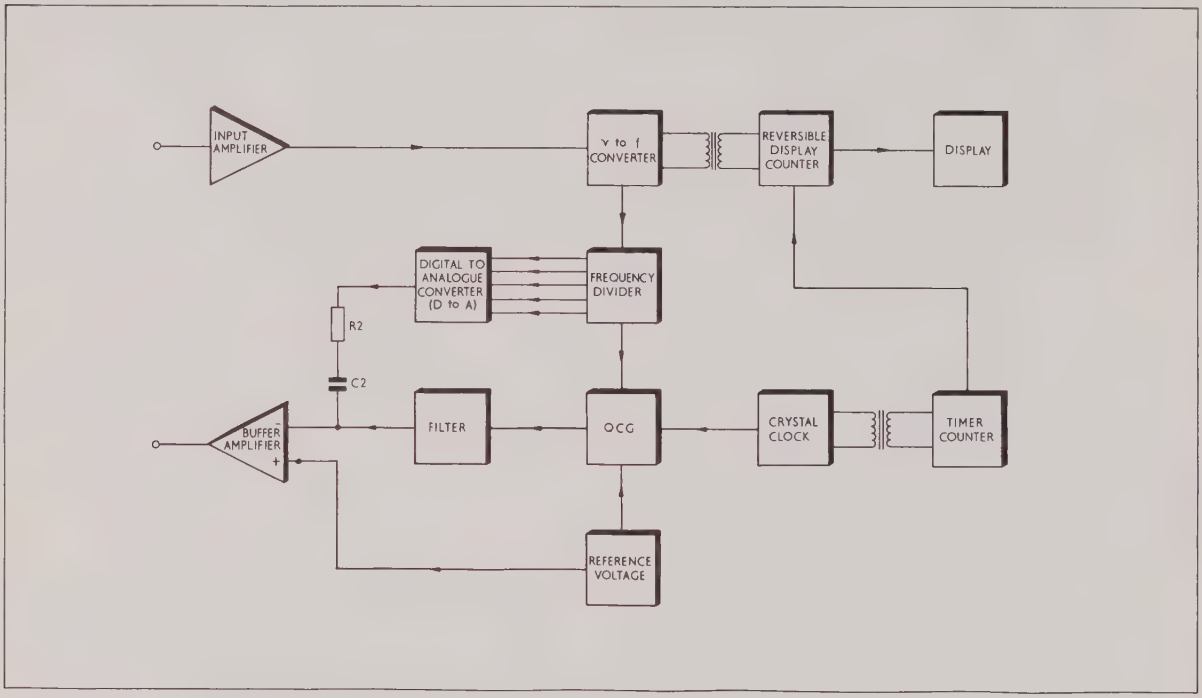


Fig. 3.9 Realisation of Increased Scale Length

At low QCG rates the ineffective smoothing by the filter still occurs, but a correction is derived from a Digital to Analogue (D to A) Converter and applied at the filter output. The output from the D to A converter is equal and opposite to the output of the filter. This correction is a.c. coupled to the filter output so that the mean level is unchanged but the fluctuations in level are smoothed out as shown in Fig. 3.10.

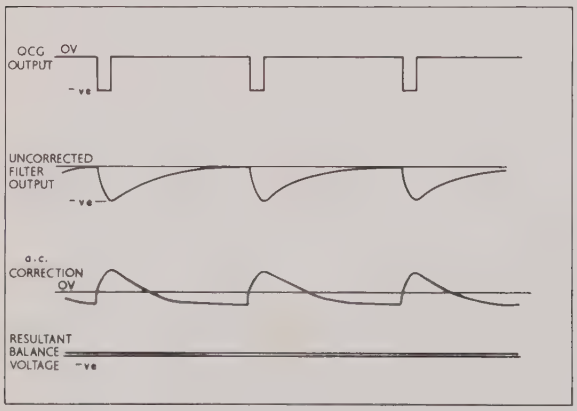


Fig. 3.10 Effect of a.c. Correction

Although the correction is applied at all QCG rates, its significance is greatest as the period between pulses approaches the filter time-constant.

Use is made of the crystal clock and reference source, required by the QCG, for deriving a time source for the timer and an offset voltage for the buffer amplifier.

AUTO-CAL

In any high resolution voltmeter, if the displayed reading is to be relied upon, then calibration at regular intervals is necessary. Performed manually, repetitive calibration is a time consuming exercise, therefore a voltmeter which calibrates itself automatically is required.

Because effects of temperature, humidity and age cause a variation in the position and slope of the voltmeter characteristic, calibration must consist of deriving correction increments which re-adjust both slope and position.

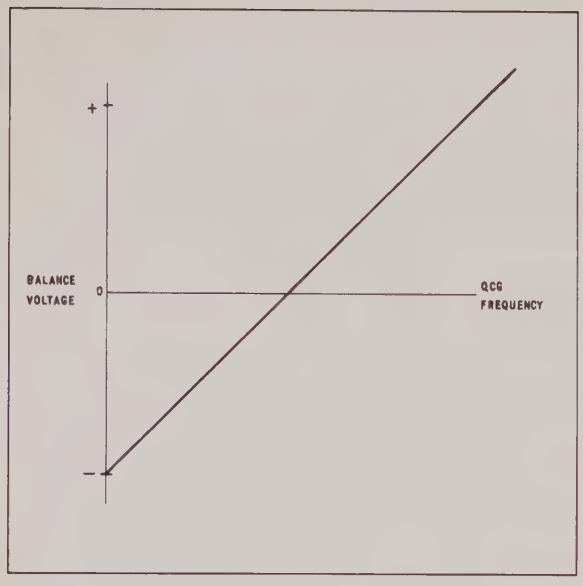


Fig. 3.11 Voltmeter Characteristic

Because the characteristic is linear, these increments need be determined only by calibrating at the extremes. Variation of the buffer amplifier offset voltage varies the position of the characteristic as in Fig. 3.12.

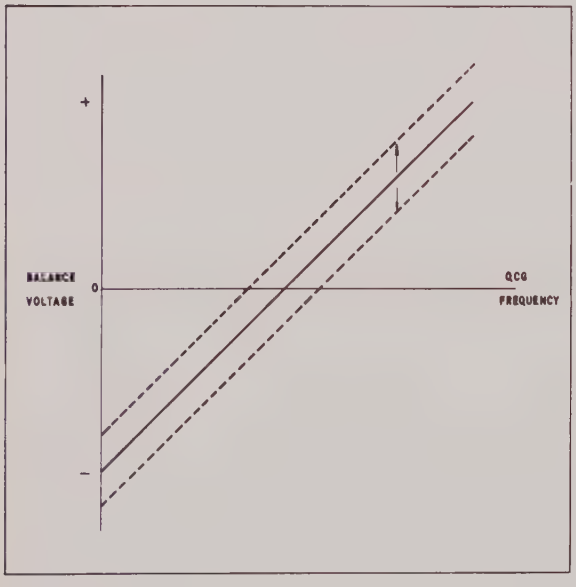


Fig. 3.12 Effect of Varying Offset

Similarly, if the amount of charge (Q) contained by each QCG pulse is varied (by varying the pulse amplitude), then the slope is adjusted as in Fig. 3.13.

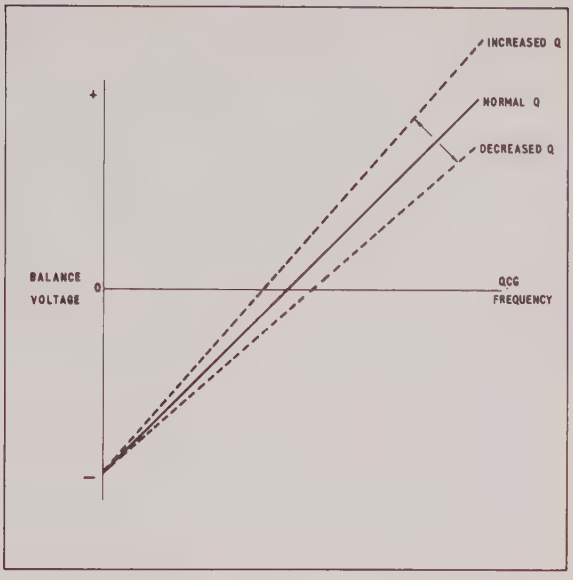


Fig. 3.13 Effect of Adjusting Q

Thus calibration must adjust the offset magnitude and the pulse amplitude. A condition of calibration is that correction at one extreme must have little or no effect at the other extreme. This condition is satisfied when calibrating the positive extreme, because correction at this end consists of slope correction only. However, adjustment of the offset at the negative extreme produces an identical change at the positive extreme. This problem is overcome by simultaneously introducing proportional slope correction (which has little effect at negative end), so that, as the offset is adjusted at the negative extreme, slope and offset correction at the positive extreme effectively fix this point as in Fig. 3.14.

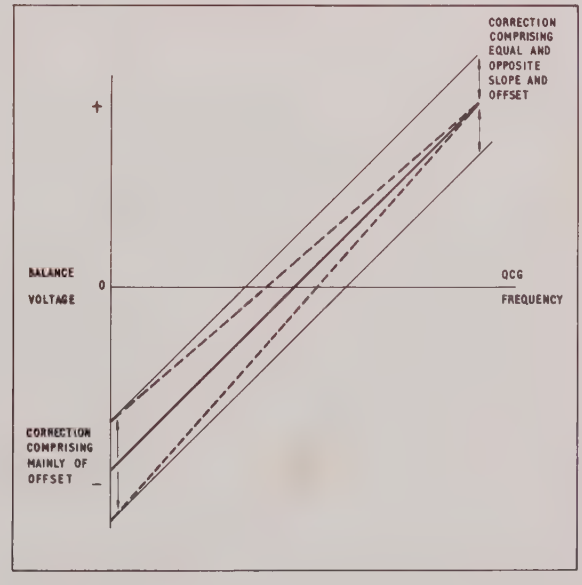


Fig. 3.14 Calibration at Negative Extreme

These increments are derived and applied automatically as shown in Fig. 3.15.

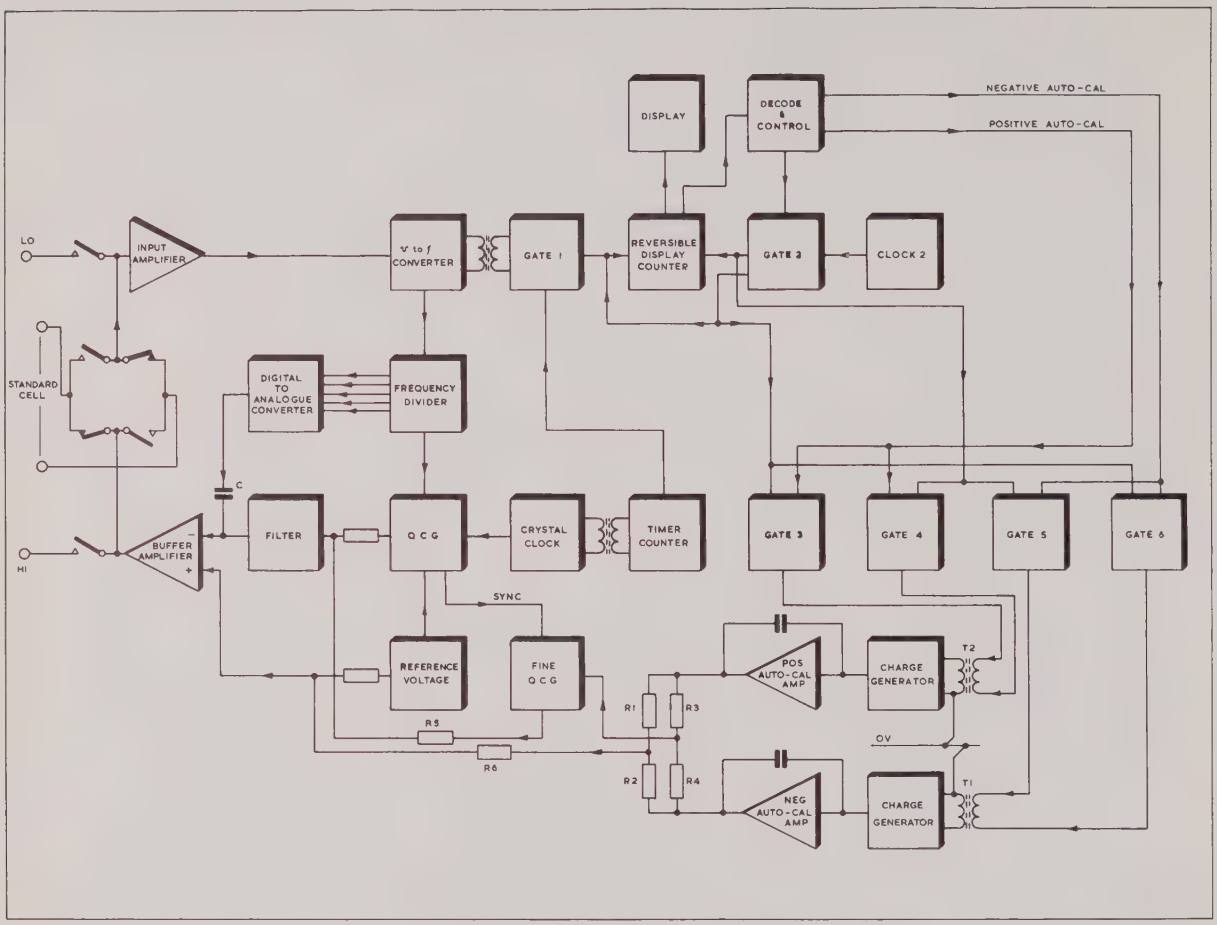


Fig. 3.15 Auto-Cal System

With the unknown voltage disconnected, a reference voltage is connected to the input terminals and its e.m.f. measured. At the end of the measurement period the Decode and Control circuit determines the number of pulses (if any) required to correct the count so that it is equal to the reference voltage. If correction is required, GATE 2 is opened to enable pulses from CLOCK 2 to either add or subtract (COUNT UP or COUNT DOWN) pulses from the total until the correct value is reached. When calibrating the negative extreme, GATES 5 and 6 are opened by the NEGATIVE AUTO-CAL command, from DECODE & CONTROL, and the CLOCK 2 pulses applied to either one end or the other of T1. The application of either the COUNT UP pulses to one end of the primary or COUNT DOWN pulses to the other end, produces either positive or negative pulses respectively at T1 secondary. These positive or negative pulses are translated by the CHARGE GENERATOR into positive or negative amounts of charge, which are summed with the charge already stored on C1, to produce an analogue of the digitally derived correction. Offset correction is derived from the junction of R1 and R2 whilst QCG amplitude correction is derived from the junction of R3 and R4. Offset correction is summed directly with reference offset but QCG correction is synchronously chopped at QCG frequency, by FINE QCG, and then summed with the QCG output.

It is apparent that interaction between negative and positive correction occurs but this is overcome by calculating the values of R1, R2, and R3 and R4 so that interaction is progressively reduced with each successive calibration.

SERIES MODE REJECTION

The term series mode interference refers to any unwanted a.c. or d.c. which appears in series with the signal to be measured. It may arise as a part of the source as in Fig. 3.16a. where the signal to be measured (e) and the interference (Vs) are superimposed upon one another, or as a pick-up on the connecting leads as in Fig. 3.16b

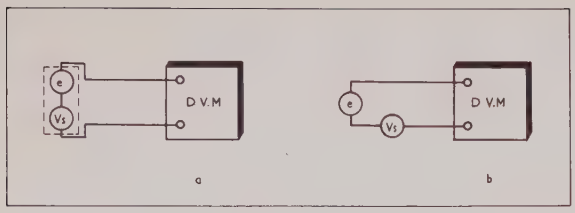


Fig.3.16 Series Mode Interference

When Vs is d.c. there is no way of causing the voltmeter to ignore it, but it may be possible if Vs can be identified, to back-off a few micro-volts by using the nV OFFSET control, or subtract the error from the reading. It is more usual though, that Vs is an a.c. source, the most prevalent being mains derived (either 50Hz or 60Hz, and their harmonics) for this reason the LM1490 has been designed to read the mean value of the input (the d.c. component) and effectively ignore the a.c. The integrating action of LM1490 is illustrated in Fig.3.17 where v to f converter pulses are continually produced at a rate proportional to the input.

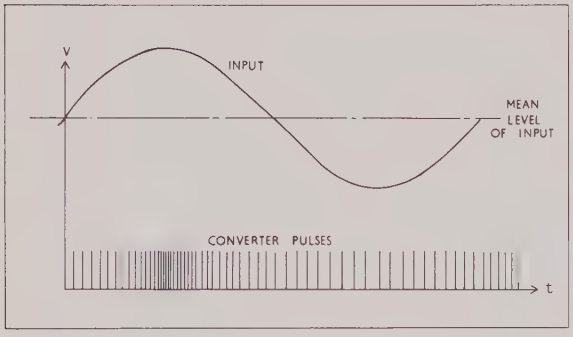


Fig.3.17 Averaging Effect

The result of counting them over a 20mS, 200mS or 2S time interval (all of which are available in LM1490) is, that the average value of any 50Hz, 5Hz or 0.5Hz components, (and their harmonics) respectively, is zero.

LINE SYNC – This facility provides additional rejection of mains derived interference by controlling integration to compensate for changes in mains frequency. The time source from which the integration periods are derived is crystal controlled and the 20mS, 200mS and 2S integration periods therefore give infinite rejection of 50Hz and its harmonics. However, the frequency of the mains can vary as much as 1% from the nominal 50Hz, thus when interference of this nature is present, incomplete rejection will occur if integration does not take this into account. To compensate for variations of line frequency, integration is performed twice in the manner described below. The process is synchronised such that the start of the first integration period is coincident with the point at which the supply passes through its own zero in a positive direction, and ends after a pre-selected integration time (2mS, 20mS, 200mS or 2S). The resulting pulses from the v to f converter are halved in number before being counted, and retained by the voltmeter. The start of the second integration period is then synchronised to coincide with the point at which the supply passes through its own zero in a negative direction, and ends after the preselected integration time. The v to f converter pulses are halved before being added to the previous total. The result is a display of the d.c. component of the input signal.

Fig. 3.18 Illustrates the principle, for an integration time ($t_1 = t_2$ = 20mS) of 20mS.

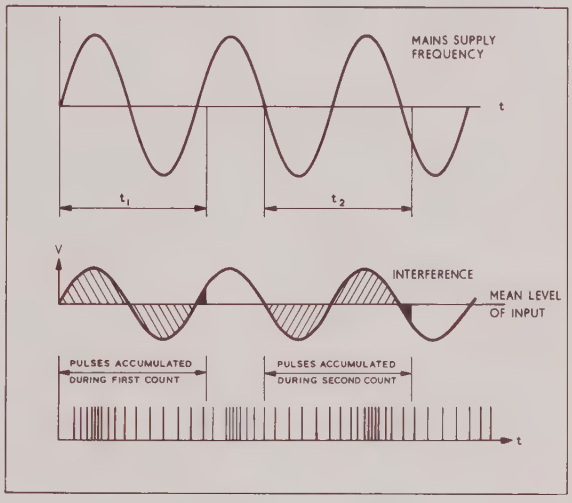


Fig.3.18 Line Synchronised Integration

COMMON MODE REJECTION

The input circuits of the LM1490 are contained in a totally screened compartment which is isolated from mains earth. Connection is made to this compartment and is available at the input connector as GUARD. This arrangement enables interference signals, developed across the signal source resistance by common mode current, to be minimised.

TWO TERMINAL MEASUREMENT

For normal laboratory work, sufficient a.c. and d.c. common mode rejection will be obtained using the two terminal cable supplied. The Lo lead is connected to GUARD inside the signal lead.

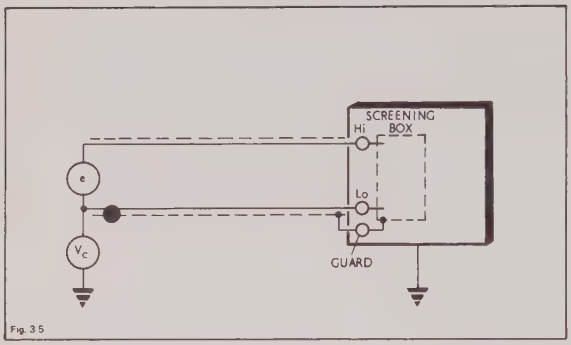


Fig.3.19 Two Terminal Measurement

THREE TERMINAL MEASUREMENT

Where the source of common mode voltage can be identified rejection can be increased, for both a.c. and d.c. common mode, by using a three terminal lead. In this cable the GUARD is also available (with Hi and Lo) so that it can be connected to the source of common mode. This arrangement provides a by-pass route for the common mode current thereby preventing it from setting up a series mode voltage across the Lo lead resistance.

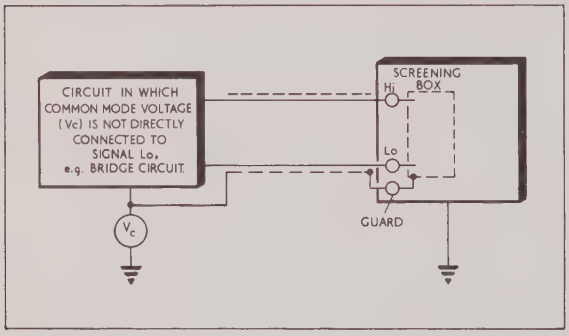


Fig.3.20 Three Terminal Measurement

A screened cable (Solartron Part No. 359900020) is available, as an extra, for three terminal measurement.

CIRCUIT DESCRIPTION

INPUT AMPLIFIER (POSITION 21)

The input amplifier is a low noise, drift corrected d.c. amplifier providing an open loop gain of >160dB at d.c. falling at 20dB/decade to unity gain at 350kHz. Fig. 3.21 is a block diagram of the input amplifier arrangement and illustrates the sections which are contained in the amplifier.

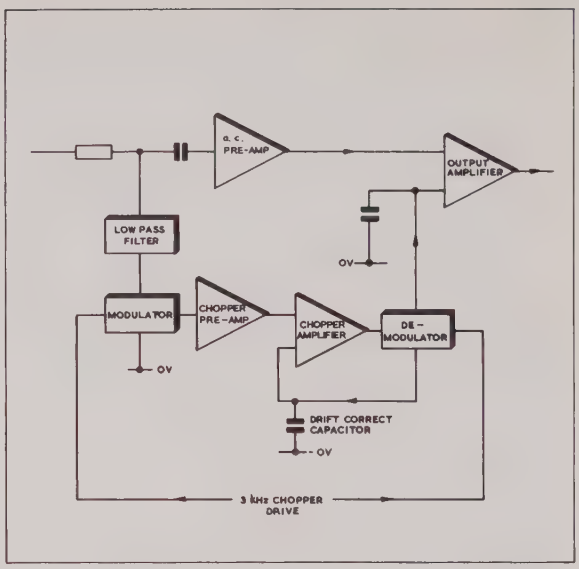


Fig.3.21 Input Amplifier – Block Diagram

D.C. and low frequency signals are transmitted via the chopper channel, while the higher frequencies pass via the a.c. pre-amp, with crossover at the output amplifier occurring at approximately 300Hz.

R1, C2 and R11 form the low pass filter (T Section), mentioned in the block diagram, which ensures that only d.c. and low frequency signals appear at the chopper, and prevents feedback of chopper spikes to the input terminals.

MODULATOR AND DEMODULATOR PHASING

Consider the modulator as a switch which alternately connects and then disconnects the chopper pre-amplifier input to 0V, and the demodulator as a change-over switch which alternately connects the chopper amplifier output to the drift correct capacitor and then to the output amplifier.

The phasing of the two switches is such that when the input signal is not connected to 0V, the chopper amplifier output is connected to the drift correct capacitor. Because of the differential nature of the chopper amplifier a balance condition will occur when the current flowing into the drift correct capacitor is zero. At this point the two input voltages are equal. However, the voltage stored on the drift correct capacitor is composed of signal and an amplifier drift component.

When the input is short circuited to 0V the demodulator connects the chopper amplifier output to the output amplifier. The differential chopper amplifier is unbalanced and the voltage stored on the drift correct capacitor defines a charging current into C9.

CHOPPER (MODULATOR)

The chopper VT14 is a twin gate MOS Field Effect Transistor which, when conducting, effectively provides a low impedance path between the low pass filter output and 0V. In the off state the impedance from the filter to 0V is so high as to leave the signal appearing at the junction of R11 and C12 unmodified.

Chopper drive derived from the emitter coupled multivibrator (VT12 and VT13) is applied to gate one (G1) of VT14 via the differential switch VT9/VT10. The switching characteristic of VT14 is quite sharp but the d.c. bias at the switching point may be in the range -1 to -4 volts. RV2 provides a preset d.c. bias for G1 and allows the drive waveform to be reduced to approximately 0.6 volts p-p. Antiphase chopping waveform is applied to gate two (G2) to minimise chopping spikes. RV1 is adjusted for minimum spike amplitude at TP2. The ideal level to which the signal is chopped is 0V, but this can be modified by inserting an offset at the junction R46 and R47, to compensate for small external, or internal, emfs which cause zero error. This offset is derived from the nV OFFSET circuitry of position 17.

CHOPPER PRE-AMPLIFIER

The chopper pre-amplifier is the feedback pair VT3/VT4, with a gain of 40 (approximately) defined by R16 and R18 The FET (VT3) at the input is a low noise device, arranged to present optimum noise impedance coupling to VT4.

CHOPPER AMPLIFIER

The Chopper amplifier comprises the differential amplifier IC2 and the output stage VT5 and VT6. VT6 is connected as a constant current source acting as load for VT5.

DEMODULATOR

The demodulator comprises two FET switches, VT15 and VT16, which are driven in anti-phase by the differential switch VT7/VT8. Drive for the switch is from the emitter coupled oscillator VT12/VT13. C17 at the differential input to IC2 is the drift correct capacitor, and C9, at the output amplifier IC1, is a demodulating capacitor which averages the d.c. referenced square-wave from VT15.

A.C. PRE-AMPLIFIER

Like the chopper pre-amplifier, the a.c. pre-amplifier is a feedback pair which incorporates a low noise FET at the front end. R6 and R4 define a gain of 10.

OUTPUT AMPLIFIER

The output amplifier IC1 is a differential amplifier with a gain (at d.c.) of 80 (approximately) defined by R9 and R8. VTs17 and 18 and MR9 are an overload catching network which starts to conduct when the output moves more than about 2V from its working point and clamps it to the input.

The back to back diodes MR6 and MR7 limit any overload at the input and thus prevent the amplifier from leaving its linear range, which ensures the fastest possible recovery from overload.

VOLTAGE TO FREQUENCY CONVERTER (POSITION 23)

The output from the input amplifier is fed to the ramp generator VT4O, VT39 and C52 via pin 12. C52 charges up and a ramp is developed at the collectors of VT40 and VT39. As the ramp approaches 4V, VT45 conducts causing VT44 to cut off. The potential at the junction of R123 and R112 falls and VT41 conducts to discharge C52 and reset the ramp generator. With the generator reset VT45 cuts off causing VT44 to conduct and cut off VT41 so that the procedure may be repeated.

The pulses developed at VT41 collector are applied to the counting circuits of the voltmeter via T2 and to a divide by thirty-two stage (IC1-IC5) via R110.

The output of each bistable is terminated via binary weighted resistors at the base of emitter follower VT43. These resistors (R117, R120, R122, R127, R130) together with R51, R52, R55 and R57 (sheet 2) form a digital to analogue converter the output of which is a staircase waveform.

This staircase waveform is applied to the QCG via emitter follower VT43 and pin 11.

4 BIT MEMORY (POSITION 23)

Four bistables VT20/VT21, VT22/VT23, VT24/VT25 and VT26/VT27 comprise the 4 bit memory. Each bistable collector is clamped to the 11 volt rail, derived from MR21 by diodes MR22 - MR29 to achieve logic levels of 0V and +11.5V.

Normal Operation

MR30 – MR33 and R44 – R47 form a detector which controls the RESET command/inhibit elements VT18 and VT28. If 0V is detected at the cathodes of two or more of these diodes, the base potential of VT18 is reduced sufficiently to cause VT18 to conduct and VT28 to cut off so that a RESET pulse is commanded from the QCG. Because of the continuously recycling mode of operation of the memory there is no defined start or finish point to the sequence, therefore consider the memory to be in the

state shown in Table 3.1 Step I.

STEP	VT27	VT26	VT25	VT24	VT23	VT22	VT21	VT20
1	+11.5V	0V	0V	+11.5V	0V	+11.5V	0V	+11.5V
2 Set	+11.5V	0V	+11.5V	0V	0V	+11.5V	0V	+11.5V
3 Reset	0V	+11.5V	+11.5V	0V	0V	+11.5V	0V	+11.5V
4 Set	0V	+11.5V	+11.5V	0V	+11.5V	0V	0V	+11.5V
5 Reset	0V	+11.5V	0V	+11.5V	+11.5V	0V	0V	+11.5V
6 Set	0V	+11.5V	0V	+11.5V	+11.5V	0V	+11.5V	0V
7 Reset	0V	+11.5V	0V	+11.5V	0V	+11.5V	+11.5V	0V
8 Set	+11.5V	0V	0V	+11.5V	0V	+11.5V	+11.5V	0V

Table 3.1

MR50 is reverse biased by 1V but MR51, MR49 and MR48 are all reverse biased by 6.5V approximately.

A 5V negative going SET pulse, generated after every 32 v/f pulses, is applied to the SET line via R135, forward biasing MR50 via C34, causing VT25 to cut off and VT24 to conduct. 0V is now detected at the cathodes of MR32 and MR33 thus satisfying the requirements for RESET command.
After a short delay ($<4\mu S$) the RESET pulse is applied to the RESET line, forward biasing MR55 via C34 causing VT26 to cut off and VT27 to conduct. MR33 is reverse biased satisfying the requirements for RESET inhibit.

MR49 is now reverse biased by 1V and MR51, MR50 and MR48 by 6.5V therefore the next SET pulse forward biases MR49 causing VT23 to cut off and VT22 to conduct. RESET command requirements are satisfied by 0V at the cathodes of MR31 and MR32. The next RESET pulse forward biases MR54 causing VT24 to cut off and VT25 to conduct. MR32 is reverse biased satisfying the RESET inhibit requirements.

The memory has now completed Step 5 of Table 3.1 and it is apparent that the next SET and RESET pulses will reverse the states of bistables VT21/VT20 and VT23/VT22 respectively.

Overload Conditions
MR36 - MR39 and R49 R50, R53 and R54 form a detector which controls v/f overload clamp transistors VT19, VT29 and VT42. If +11.5V is detected at the cathodes of 3 or all of these diodes, the base potential of VT19 is sufficiently positive to cause VT19 to cut off, VT29 to conduct and VT42 to conduct. VT42 conducting prevents pulses being generated by the v/f converter.

Under overload conditions the v/f converter pulse rate increases to a frequency sufficiently high as to allow a second SET pulse to be generated before the first RESET pulse is received.

Consider the memory to be at Step 8 of Table 3.1

STEP	VT27	VT26	VT25	VT24	VT23	VT22	VT21	VT20
8 Set	+11.5V	0V	0V	+11.5V	0V	+11.5V	+11.5V	0V
9 Set	+11.5V	0V	+11.5V	0V	0V	+11.5V	+11.5V	0V
10 Reset	+11.5V	0V	+11.5V	0V	0V	+11.5V	0V	+11.5V
11 Set	+11.5V	0V	+11.5V	0V	+11.5V	0V	0V	+11.5V
12 Reset	0V	+11.5V	+11.5V	0V	+11.5V	0V	0V	+11.5V

Table 3.1 Continued

The next SET pulse is generated before a RESET and the memory adopts the states of Step 9. +11.5V is now detected by MR37, MR36 and MR39 and the v/f converter is inhibited.

The RESET pulse is now generated causing VT20 to cut off and VT21 to conduct. The inhibit is removed from the v/f converter. Although RESET command is still present the next SET pulse appears before RESET is generated and the states of Step 11 are adopted. The v/f converter is inhibited and the next RESET pulse causes the memory to adopt the states of step 12.

For the period that an overload is present the v/f converter is controlled by the memory in the above fashion so that the number of output pulses to the counting circuits is restricted to the minimum number required to give a full scale reading. Removal of the overload causes the memory to return to the normal operating mode.

QUANTISED CHARGE GENERATOR (QCG) POSITION 22)

Two bistables VT3/VT4 and VT6/VT7, are used to generate RESET pulses for the 4 Bit Memory and control the action of the emitter switch VT12 and VT13.

The two bistables are interlocked by diodes MR12, MR14 MR15 and MR23 in such a way that VT6/VT7 cannot turn over until VT3/VT4 has changed state. VT3/VT4 cannot change state until the inhibit at the anode of MR11 is removed by reverse biasing MR7. Therefore, the initial conditions prior to a pulse command from the 4 Bit Memory are:-

VT3 collector -9V
VT4 collector +2V
VT6 collector -9V
VT7 collector +2V

The pulse command cuts off VT2 causing the collector potential to rise sufficiently to reverse bias MR7. A $\overline{\text{CLOCK}}$ pulse drives a positive spike through MR11 onto the base of VT4. VT4 conducts, clamping the junction of MR20 and C17 via MR14 and issuing a RESET pulse to the 4 Bit Memory via C14. VT2 conducts and re-clamps the junction of MR11 and C16 by reverse biasing MR15. VT3 cuts off releasing the clamp from the junction of MR22 and C20. A CLOCK pulse now drives a positive spike through MR22 onto VT7 base causing VT7 to conduct. VT6 cuts off, reverse biasing MR12 and removing the clamp from the junction of MR9 and C12. The next $\overline{\text{CLOCK}}$ pulse drives a positive spike through MR9 onto the base of VT3. VT3 conducts restoring the clamp to the junction of MR22 and C20 by forward biasing MR15. VT4 cuts off removing the clamp from the junction of MR20 and C17. The next CLOCK pulse drives a positive spike through MR20 onto VT6 base, causing VT6 to conduct and clamp the junction of MR9 and C12 by forward biasing MR12. VT7 cuts off and the circuit is reset.

Further CLOCK and $\overline{\text{CLOCK}}$ pulses have no affect on the circuit until the next pulse command appears.

The width of the pulses to be used for feedback is therefore defined as one CLOCK period (3.125μS).

As VT7 collector goes negative VT8 emitter follows suit causing VT12 to cut off and VT13 to conduct. The junction of VT12 emitter and VT13 emitter assumes a potential, within a few millivolts of VT13 collector, referenced by zener diode MR34. This diode has a temperature coefficient which approaches zero and is supplied from a constant current source VT10, VT11, VT14 and VT15. At the end of the pulse, as VT7 collector potential rises to +2V, VT8 emitter potential rises causing VT12 to conduct and VT13 to cut off. The emitter junctions are now clamped to 0V. Thus the output from the junction of VT12 emitter and VT13 emitter is a negative pulse of closely defined width and amplitude. The pulse is integrated by the network comprising R39 and C27 and summed with the staircase waveform produced by the digital to analogue converter to produce a small d.c. voltage.

The staircase waveform is a.c. coupled to the uncorrected feedback via R50 and C26 to effect greater smoothing without altering the mean d.c. level.

This d.c. level is adjusted slightly by the output from the two AUTO-CAL amplifiers which is chopped at QCG frequency by VT17, via R43, R44 and R41 to provide final correction before being applied to the Buffer Amplifier.

The reference level offset to the Buffer Amplifier is derived from the reference zener MR34 via the potential divider network formed by R42 and R45. Offset correction derived from the AUTO-CAL amplifiers via R46, R47 and R48 is applied to this reference.

POSITIVE AUTO-CAL AMPLIFIER (POSITION 23)

The purpose of this amplifier is to store the feedback offset and feedback reference correction components derived during the AUTO-CALibration at high QCG rates. The amount of correction required is determined by the AUTO-CAL logic of the voltmeter and transmitted in digital form via two transformers, to the AUTO-CAL amplifier, where it is translated into an analogue correction voltage. The number of pulses transmitted determines the magnitude of correction required, and their polarity determines whether the correction must be added to or

subtracted from any existing correction. Positive pulses indicate addition to, negative pulses subtraction from the existing correction.

A positive pulse, of approximately 0.5μS duration, from T1 causes VT3 to conduct, reducing the potential at the junction of R!9 and R22 to approximately +8.6V. VT6 conducts causing C5 (positively charged to approximately +17V) to discharge through R20 to provide the emitter current. In an attempt to restore lost charge C5 draws current via MR4, MR3 and MR8 and in doing so forward biases them. VT3 emitter is pulled negative, maintaining conduction of VT3 whilst MR8 cathode is fixed at -2V approximately. When C5 discharges to a potential (+3.5V) sufficient to cause VT6 to cut off, MR8, MR3 and MR4 become reverse biased, cutting off VT3 by raising the emitter potential. The potential at the junction of RI9 and R20 rises, forward biasing MR10, to charge C5 via R20. While VT6 is conducting, low leakage diode MR9 is forward biased so that the charge released from C5 is transferred to C3. When VT6 cuts off MR9 reverse biases preventing C3 from discharging through VT6. Further positive pulses from T1 cause an accumulation of charge on C3. Negative pulses from T1 cause the negative charge of C1 to be transferred to C3 in identical fashion but effecting a reduction of charge on C3.

An increase in charge on C3 increases the input voltage to the 3 stage hold amplifier VT4, VT5 and VT6, causing the voltage at MR74 anode to fall and increasing the charge on C2, C7 by an amount equal to the additional charge on C3. The change in output voltage is only one hundredth (approx) of the change in input voltage.

A Field Effect Transistor is used in the input of this amplifier so that very little current is drawn from C3 and therefore accurate correction is maintained between AUTO-CAL runs.

The negative AUTO-CAL amplifier (position 22) operates in identical fashion to the positive AUTO-CAL amplifier.

CLOCK (POSITION 22)

The 320kHz MAIN CLOCK is generated by a crystal controlled class "C" oscillator comprising VT28, T1 C39 and XL1. The output from VT28 is applied via C41/R63, to the bases of VT30 and VT29. Thus, as each current pulse occurs VT29, VT31 and VT33 conduct while VT30 and VT32 are cut-off.

The amplitude of the output waveforms is limited to 0V and -6V by clamp diodes.

Fig. 3.22 illustrates the outputs from VT32 and VT33 collectors.

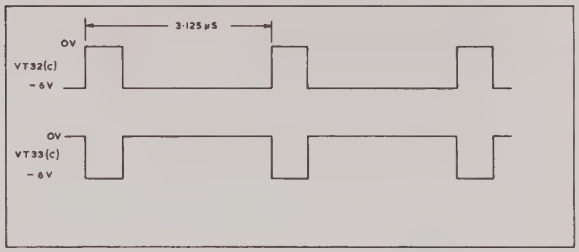


Fig.3.22 Clock Waveforms

BUFFER AMPLIFIER (POSITION 20)

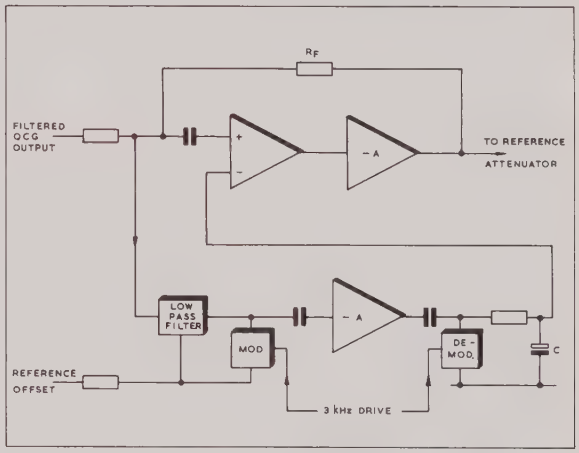


Fig.3.23 Buffer Amplifier — Block Diagram

The basic arrangement of the buffer amplifier is shown in Fig. 3.23. The filtered QCG output and the reference offset are summed by chopping the QCG output to the offset. The resulting square wave is amplified and synchronously demodulated to restore it to d.c. The d.c. is applied to the inverting input of a differential amplifier whose other input is a.c. coupled to the QCG output. This arrangement eliminates the effects of drift of the amplifier stages.

Overall negative feedback is effected by R_F

CHOPPER (MODULATOR)

The chopper drive, from the floating power supply, is applied to the base of VT6 via MR6 and R24. When VT6 conducts, R25 provides a low impedance path between the low pass filter (R9, C8 and R21) output and the reference offset.

To eliminate chopper spikes which may appear at the output of the chopper amplifier (TP2), antiphase chopping waveform is applied to the emitter of VT6 via C9, R20 and C11 and C11 adjusted until the spikes at TP2 are minimised.

SYNCHRONOUS DEMODULATOR

The output from the amplifier is d.c. restored by C21 and VT10, which is switched synchronously with VT6 such that when VT6 conducts so does VT10. The d.c. referenced square wave is filtered by R40 and C22 and the resulting mean d.c. level applied to the inverting input of the differential amplifier.

INPUT SWITCHING (POSITION 17)

Reference Attenuator

On all ranges the available output from the Buffer Amplifier is $\pm$20V nominal. The reference attenuator provides attenuation ratios of unity, 10:1, 100:1, and 1000:1 to provide the correct balance voltages on the 20V, 2V, 200mV and 20mV ranges respectively. Figs. 3.24 to 3.27 illustrate the arrangements selected for the above ranges.

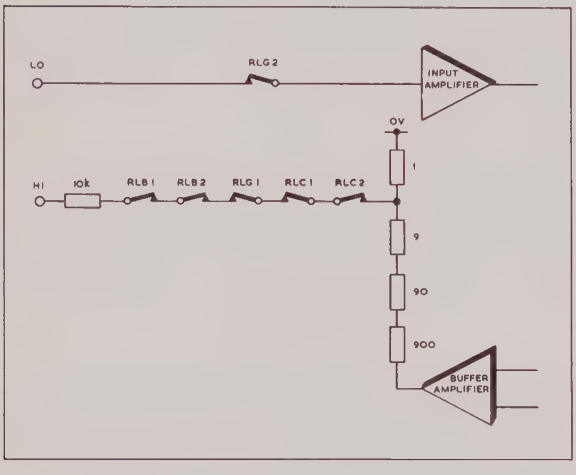


Fig.3.24 20mV Range

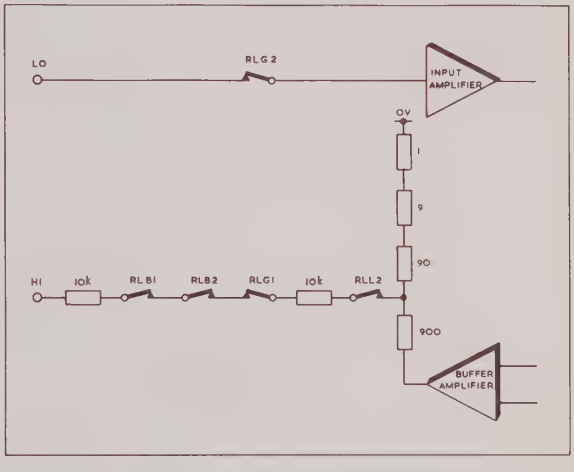


Fig.3.25 2V Range

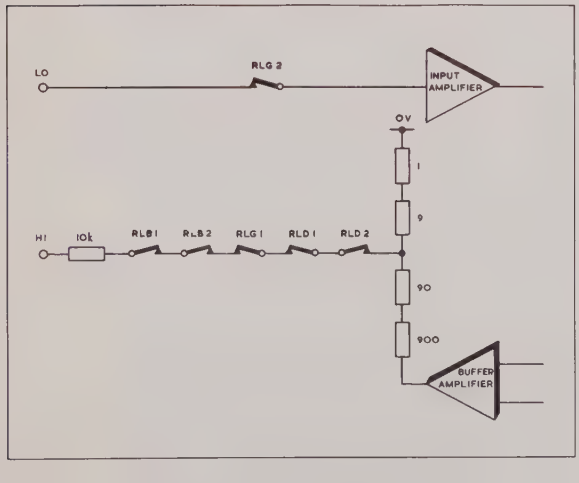


Fig.3.26 200mV Range

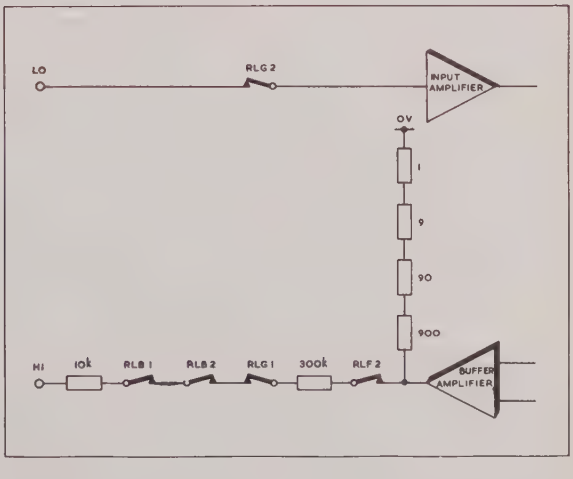


Fig.3.27 20V Range

200V AND 1000V RANGES

A 100:1 input attenuator reduces the input signal so that it can be accommodated by the 2V and 20V ranges when the 200V and 1000V ranges are selected, respectively.

Fig. 3.28 and 3.29 illustrate both conditions.

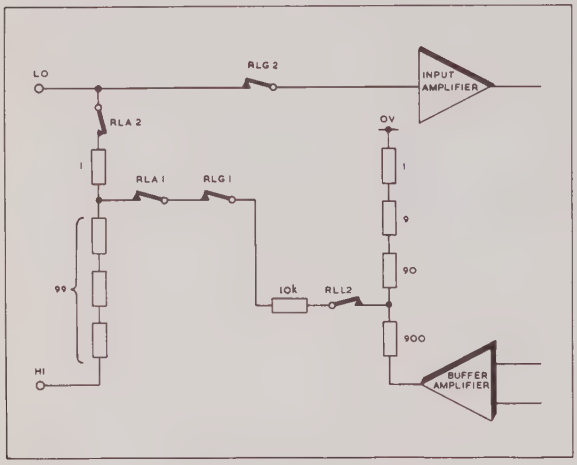


Fig.3.28 200V Range

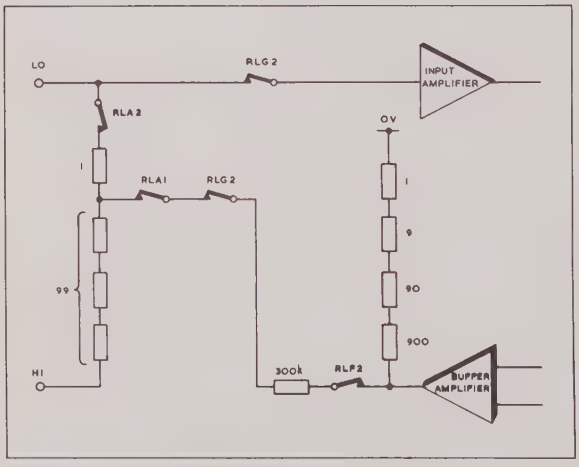


Fig.3.29 1000V Range

FILTER

When FILTER is selected RLH is energised and connects a single section low pass filter with a 100mS time constant. On the basic ranges two 4.7μF capacitors in parallel (C2 and C5) are connected from R1 (10kΩ) to the Lo input terminals. When on the 200V or 1000V ranges a 1μF capacitor C1 is connected across R6 (100k).

nV OFFSET

The nV OFFSET control is a bridge attenuator network with coarse adjustment effected by linking R29 to either A, B, C, D, E, F or G and fine adjustment by RV1, the nV OFFSET potentiometer. The table below shows the range of adjustment at pin 17, for each linking arrangement.

LINK R29 TO:-	OUTPUT RANGE FROM	TO
A	+5.6V	+2.8V
B	+4.2V	+1.4V
C	+2.8V	0V
D	+1.4V	-1.4V
E	0V	-2.8V
F	-1.4V	-4.2V
G	-2.8V	-5.6V

These ranges are reduced by 10 000:1 by the potential divider comprising R47 and R46 (Position 21), before summing at the source of VT14 (Position 21).

CONTROL LOGIC (POSITION 10)

MANUAL

When the MANUAL push button is depressed, the AUTO button is released and a negative pulse 'sets' SAMPLE bistable IC15 so that IC15(16) assumes a Lo and IC15(9) assumes a Hi.

The first available 10kHz pulse triggers WAIT bistable IC16, via IC14b, so that IC16(9) assumes a Hi and primes IC5a. The leading positive edge of the first available MAIN CLOCK pulse, from VT2, triggers STAT 1 bistable IC4 via IC5c and RESET bistable IC6 via IC5b andIC5a and IC5d. IC4(6) assumes a Lo state which inhibits the POWER STAT gates IC17a and IC17b. IC6(6) assumes a Hi state which resets IC20 and IC21 via IC13c (primed by Hi from IC12(6), the DIVIDE BY TEN stage (IC8, IC9 IC10 and IC11) via IC7a and resets the TIMER COUNTER (position 7) and the DISPLAY COUNTERS (positions 3, 4, 6, 8, 9, 11). IC6(9) assumes a Lo state which resets

AUXiliary bistable IC1 so that IC1(9) assumes a Lo.

One MAIN CLOCK period (3.125μs) later, the positive edge of MAIN CLOCK:-

i) triggers READY bistable IC2, via IC5b, so that IC2(6) assumes a Hi state.

ii) triggers RESET bistable IC6 via IC5b, IC5a and IC5d so that IC6(6) assumes a Lo state. IC2(6) Hi, activates IC14a so that WAIT INHIBIT (Lo) is generated which resets WAIT bistable, IC16 and primes the first bistable in the TIMER COUNTER (IC1) so that MAIN CLOCK pulses can be accumulated to define the INTEGRATION TIME. IC16 reset, inhibits IC5a. IC6(6) Lo, removes RESET from the timer and display counters, IC20, IC21 and the DIVIDE BY TEN stage.

The lagging negative edge of the same MAIN CLOCK triggers COUNT bistable IC3, (so that IC3(6) assumes a Hi state and IC3(9) assumes a Lo state) and triggers the first stage of the TIMER COUNTER . The Lo from IC3(9), inhibits IC5c and holds RESET bistable IC6 in the RESET state.

The Hi from IC3(6) enables ½ BIT BISTABLE, IC20, to be triggered by v-f converter pulses from VT1. The pulses are halved in frequency by the ½ BIT BISTABLE and applied via IC19a and IC19b, to the junction of IC19b(8), IC8(2) and IC7b(4).

The path taken by the v-f converter pulses from this point is determined by the INTEGRATION TIME selected.

2mS: converter pulses are transferred to the hundreds decade counter (position 8) via IC7b (primed by X10 being Hi when X10 TIME MULT. facility not in use) and IC18b (primed by 2mS CONTROL, from IC15b in the TIMER COUNTER).

20mS: converter pulses are transferred to the tens decade counter (position 9), via IC7b and IC18c (primed by 20mS CONTROL from IC21a in the TIMER COUNTER).

200mS: converter pulses are transferred to the units decade counter (position 11), via IC7b and IC18d (primed by 200mS CONTROL from IC21b in the TIMER COUNTER).

X10 TIME MULTiplier: With this facility selected the INTEGRATION TIME is increased by a factor of ten, but the number of converter pulses is reduced proportionately by the DIVIDE BY TEN stage. Table 3.2 is a truth table for this stage and shows that a Hi to Lo transition (at IC11(6)) occurs every 5,15 25, etc. input pulses. This arrangement ensures that readings are displayed to the nearest 'bit'.

INPUT PULSE	CONDITION			
	IC8(6)	IC9(6)	IC10(6)	IC11(6)
0, 10	Hi	Lo	Hi	Lo
1, 11	Lo	Hi	Hi	Lo
2, 12	Hi	Hi	Hi	Lo
3, 13	Lo	Lo	Lo	Hi
4, 14	Hi	Lo	Lo	Hi
5, 15	Lo	Lo	Lo	Lo
6, 16	Hi	Lo	Lo	Lo
7, 17	Lo	Hi	Lo	Lo
8, 18	Hi	Hi	Lo	Lo
9, 19 etc.	Lo	Lo	Hi	Lo

Table 3.2 Divide by Ten Truth Table

The output from IC11(6) is applied to the appropriate decade counter via IC18a (primed by X1 Hi when X10 TIME MULTiplier selected) and either IC18b, IC18c or IC18d.

At the end of the count period the output from the TIMER COUNTER assumes a Lo state which triggers AUXiliary bistable IC1 so that IC1 (9) assumes a Hi state. The positive edge of the next MAIN CLOCK triggers READY bistable IC2 via IC5b, so that IC2(6) assumes a Lo. IC2(6) Lo, removes WAIT INHIBIT from IC16 via IC14a and inhibits the first stage of the TIMER COUNTER to prevent the further accumulation of clock pulses.

The lagging negative edge of the same MAIN CLOCK triggers COUNT bistable IC3 so that IC3(6) assumes a Lo and IC3(9) assumes a Hi state. IC3(6) going Lo triggers SAMPLE bistable IC15 so that IC15(6) returns Hi and IC15(9) returns Lo which prevents WAIT bistable IC16 from being triggered by 10kHz pulses. IC3(9) Hi primes IC5c. The Lo on IC3(6) prevents triggering of ½ BIT BISTABLE IC20 so that accumulation of converter pulses ceases.

The positive edge of the next MAIN CLOCK triggers STAT 1 bistable IC4, via IC5c, so that IC4(6) assumes a Hi. IC4(6) Hi triggers the STATICISE bistables in the display counters via the POWER STAT gates IC17a and IC17b, so that the display is updated.

The control logic remains in this state until the MANUAL button is depressed again when the sequence is repeated.

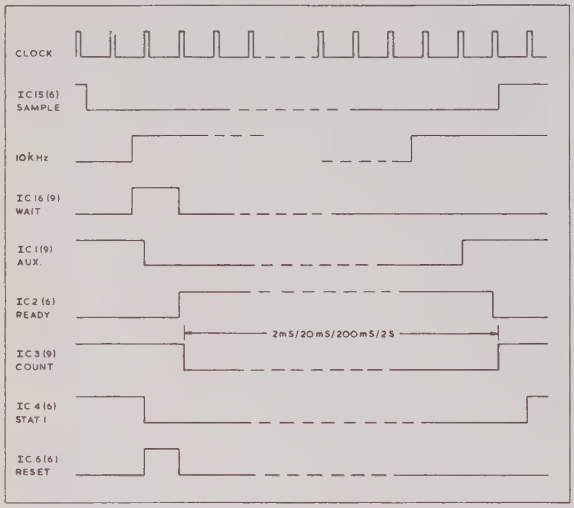


Fig.3.30 Control Timing — Manual

MANUAL LINE SYNC

Depressing the LINE SYNC push button inhibits IC14b, IC7c and IC19b. IC14b inhibited prevents 10kHz pulses from reaching WAIT bistable IC16. Instead IC7c(8) assumes a Hi which primes IC13a and IC13b so that IC16 is triggered by 50Hz and $\overline{50Hz}$ pulses derived from a generator in the power supply, which changes state as the 50Hz mains supply passes through its own mean level.

Depressing the MANUAL push button sets IC15(6) Lo and IC15(9) Hi. The first positive edge of a 50Hz pulse triggers WAIT bistable IC16 via IC13a (Primed by Hi outputs from IC7c and IC12(6)). The sequence proceeds as in MANUAL until COUNT bistable IC3 is triggered when IC3(9) going Lo triggers STAT 2 bistable IC12 so that IC12(6) assumes a Lo state and IC12(9) assumes a Hi state.

The output from ½ BIT BISTABLE IC20(6) triggers LINE SYNC ÷2 bistable so that the converter pulses are halved in quantity twice. The output from IC21 is applied to the display counters via IC19b and then as in MANUAL.

The Lo from IC12(6) inhibits IC13a and then Hi from IC12(9) primes IC13b. The outputs from IC12 also prevent SAMPLE bistable IC15 from being triggered and inhibit the POWER STAT gates IC17 a and b.

The second count is initiated by the leading positive edge of the first available $\overline{50Hz}$ pulse triggering WAIT bistable IC16 via IC13b. STAT 2 bistable IC12 is triggered by IC3(9) going Lo so that when, at the end of count, IC3(6) goes Lo SAMPLE bistable IC15 is triggered and the sequence terminates.

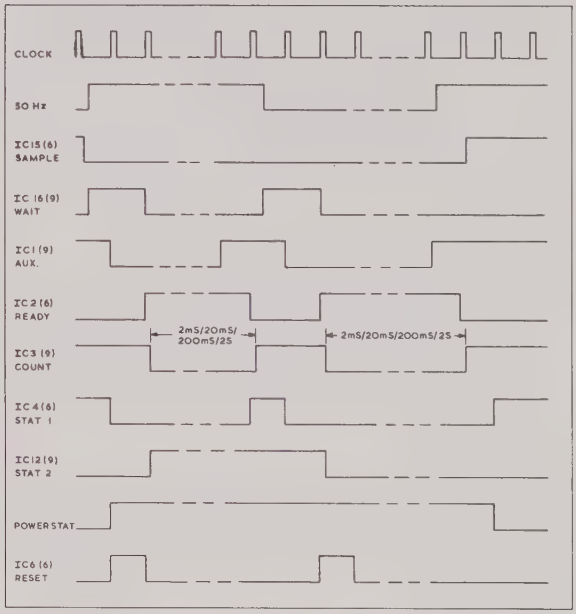


Fig.3.31 Control Timing — Manual Line Sync

AUTO

When the AUTO push-button is depressed, IC15(6) is set permanently Lo so that at the end of each count WAIT bistable can be re-triggered by 10kHz pulses via IC14b. Thus AUTO operation is repetitive MANUAL operation.

AUTO LINE SYNC

With AUTO and LINE SYNC selected, operation is repetition of the MANUAL LINE SYNC mode.

DISPLAY COUNTERS (POSITIONS 3,4,6,8,9 and 11)

The general arrangement of the display counter is shown in Fig.3.32 Reversible synchronous counters, driven by the v—f pulses, are employed for all the decades. Each stage has a decode circuit which converts the reading to decimal form for display on the front panel. The coded form is available at the rear socket, only when a fan-out unit is fitted.

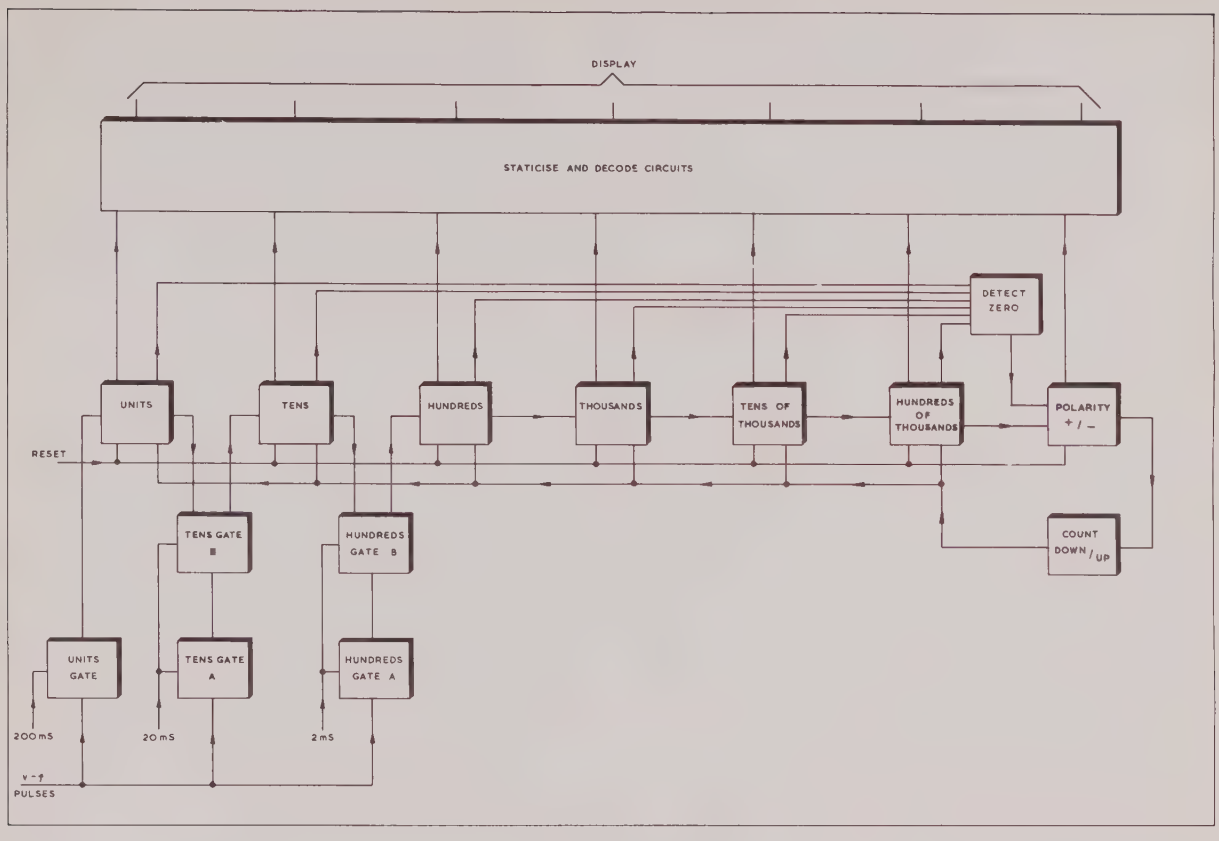


Fig.3.32 Display Counter

Before a count period the counter is reset to -255000, i.e. full scale negative. The count is started and v-f pulses from the ½ BIT BISTABLE (Position 10) initiate a count down sequence i.e. the first pulse sets the counter to -254999, the second to -254998 etc. For negative input voltages the count never reaches 000000 and polarity remains unaltered. For positive input voltages the count reaches zero, the polarity sign is reversed and count up from zero commences.

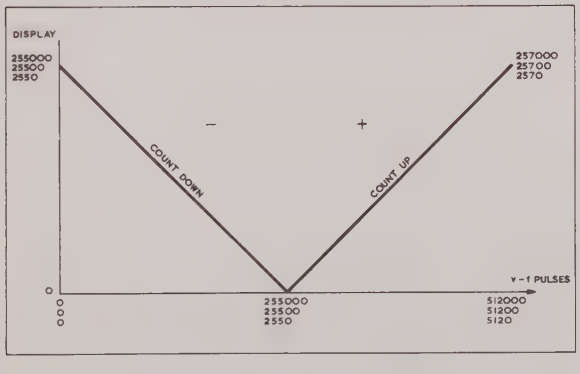


Fig.3.33 Reversible Counters Characteristic

At the end of integration the total held in the counters is transferred into the staticiser and retained until the end of the next integration period.

RESET

Prior to integration, the counters are reset to -255000 by the inverted RESET from IC6 on the control logic board. Inversion is effected by IC5b for positions 4, 6, 8, 9 and 11, and by the IC5c for position 3.

Table 3.3 shows the state of each counter after RESET.

POSITION	DECADE	1 IC14(6)	2 IC11(6)	4 IC7(6)	8 IC3(6)	
11	10^0	Lo	Lo	Lo	Lo	0
9	10^1	Lo	Lo	Lo	Lo	0
8	10^2	Lo	Lo	Lo	Lo	0
6	10^3	Hi	Lo	Hi	Lo	5
4	10^4	Hi	Lo	Hi	Lo	5

POSITION	DECADE	1 IC6(6)	2 IC8(6)	+/- IC4(6)	
3	10^5	Lo	Hi		2
3	Polarity	-	-	Lo	—

Table 3.3 Reset Truth Table

Count-Down (Position 3)
POL. bistable IC4 (Position 3) RESET gives:-
i) IC4(6) Lo
ii) IC4(9) Hi
IC4(6) Lo inhibits IC9a so that IC9a(3) is Hi
IC4(9) Hi activates IC9d (already primed by $\overline{10kHz/NORMAL}$ at Hi) so that IC9d(11) is Lo

IC9a(3) Hi provides $\overline{UP}$ to positions 4, 6, 8, 9 and 11, also to position 2. (Auto-Cal Logic)
IC9d(11) 10 primes IC7a via IC5a.

Count Down (Positions 4, 6, 8, 9 and 11)
Count down is commanded by $\overline{UP}$ control Lo, and Up control Hi. Both commands are inverted by IC9, giving Hi at IC9a(3) and Lo at IC9b(6). The Lo output from IC9b inhibits the UP Gates (IC4b, IC8d, IC4c, IC1c, IC5a and IC12a) during count down. The Hi output from IC9a, primes IC4a, IC8a, IC1a, IC1d, IC9d and IC15b during countdown.

I/P PULSES	DECIMAL COUNT	IC14		IC11					IC7					IC3					IC8b
		6	9	3&12	4	11	6	9	3&12	4	11	6	9	3&12	4	11	6	9	6
0	0	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Hi	Hi	Lo	Lo	Hi	Hi
1	9	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Hi	Lo	Lo
2	8	Lo	Hi	Hi	Hi	Lo	Lo	Hi	Hi	Hi	Lo	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Lo
3	7	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Lo	Hi	Lo
4	6	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Hi	Lo	Lo	Lo	Hi	Lo
5	5	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Lo	Lo	Hi	Lo
6	4	Lo	Hi	Hi	Hi	Lo	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Lo	Lo	Lo	Lo	Hi	Lo
7	3	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo
8	2	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Lo
9	1	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo

Table 3.4 Countdown Conditions

Carry Technique
When the total held in one decade changes from 0000 to 1001, IC15b is simulataneously inhibited via MR16 so that IC15b(8) assumes a Hi state which enables IC15a. IC15a(6) goes Lo to issue a CLOCK TO NEXT DECADE.

Detect Zero
When zero is detected (by Hi from IC8b(6) positions 4, 6, 8, 9 and 11 and also Hi from IC7d(11) position 3), IC1a on the motherboard is enabled and SETS the POL bistable IC4 (position 3) so that IC4(9) assumes a Lo state and IC4(6) assumes a Hi state.

The Hi output from IC4(6) enables IC9a (already primed by $\overline{10kHz/NORMAL}$) so that UP is Lo.

The Lo output from IC4(9) inhibits IC9d so that $\overline{UP}$ is Hi. Thus the countdown command is reversed to command count-up.

Count Up (Positions 4, 6, 8, 9, and 11)
The UP and $\overline{UP}$ commands are inverted by IC9b and IC9a respectively so that IC9b(6) assumes a Hi state and IC9a(3) assumes a Lo state.
The Lo output from IC9a(3) inhibits the DOWN Gates (IC4a, IC8a, IC1a IC1d and IC15b) during count up.
The Hi output from IC9b primes IC4b, IC8d, IC4c, IC1c IC5a and IC12a.

I/P	DECIMAL	IC14		IC11					IC7					IC3					IC8b
PULSES	COUNT	6	9	3&12	4	11	6	9	3&12	4	11	6	9	3&12	4	11	6	9	6
0	0	Lo	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Hi
1	1	Hi	Lo	Hi	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Lo
2	2	Lo	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo
3	3	Hi	Lo	Hi	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Lo
4	4	Lo	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Lo	Hi	Lo
5	5	Hi	Lo	Hi	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Lo	Hi	Lo	Lo	Lo	Hi	Lo
6	6	Lo	Hi	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Lo	Lo	Hi	Lo
7	7	Hi	Lo	Hi	Lo	Hi	Hi	Lo	Hi	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Lo	Hi	Lo
8	8	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Hi	Hi	Lo	Lo
9	9	Hi	Lo	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Lo	Lo	Hi	Hi	Lo	Hi	Hi	Lo	Lo
10	0	Lo	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Lo	Lo	Lo	Lo	Hi	Hi

Table 3.5 Count up Condition

Count Up (position 3)
0 to 1
When the counter is at zero, the outputs from IC6 and IC8 are:-

IC6(6) Lo, IC6(9) Hi
IC8(6) Lo, IC8(9) Hi

The Hi output from IC8(9) enables IC7b (primed by UP Lo, inverted by IC5b) so that IC7b output assumes a Lo and prevents IC8 changing state when triggered. Thus the first carry pulse, from the preceeding (10^4) decade triggers IC6 so that IC6(6) assumes a Hi state and IC6(9) assumes a Lo state.

1 to 2
The Lo output from IC6(9) inhibits IC7b so that IC7b output assumes a Hi state, which enables IC8 to change state when triggered. The next carry pulse triggers IC6 and IC8 simultaneously, so that IC6(6) assumes a Lo state and IC8(6) assumes a Hi state.

STATICISE

At the end of integration, bistables IC13, IC10, IC6 and IC2 (Positions 4, 6, 8, 9 and 11), are triggered by a POWER STAT command from the Control Logic. Their outputs assume the states present at their steering inputs i.e. the outputs of the counter bistables.

BIQUINARY DECODE

The outputs of the Staticise bistables are translated from 8421 BCD into decimal form to drive the numerical display tube V1.

The outputs from IC13 provide emitter gating to the display drive transistors VT1 to VT10. If the number to be displayed is odd, the output from IC13(6) is Hi and the output from IC13(9) is Lo, MR11 is reverse biased and MR12 forward biased. Thus, the only transistors which may conduct are those which drive the odd numerals i.e. VT2, VT4, VT6, VT8 and VT10.

Conversely if the number to be displayed is even, the outputs from IC13 are reversed and the only transistors which may conduct are those which drive the even numerals i.e. VTI, VT3, VT5, VT7 and VT9.

In each case (i.e. odd or even) the only transistor that will conduct is that whose base diodes are all connected to Hi outputs from the STAT bistables.

Table 3.6 lists the conditions required for display of each numeral.

NUMERAL	IC13(6) 1	IC10(6) 2	IC6(6) 4	IC2(6) 8	IC13(9) $\overline{1}$	IC10(9) $\overline{2}$	IC6(9) $\overline{4}$	IC2(9) $\overline{8}$
0	Lo*	Lo	Lo	Lo	Hi	Hi*	Hi*	Hi*
1	Hi	Lo	Lo	Lo	Lo*	Hi*	Hi*	Hi*
2	Lo*	Hi*	Lo	Lo	Hi	Lo	Hi*	Hi
3	Hi	Hi*	Lo	Lo	Lo*	Lo	Hi*	Hi
4	Lo*	Lo	Hi*	Lo	Hi	Hi*	Lo	Hi
5	Hi	Lo	Hi*	Lo	Lo*	Hi*	Lo	Hi
6	Lo*	Hi*	Hi*	Lo	Hi	Lo	Lo	Hi
7	Hi	Hi*	Hi*	Lo*	Lo*	Lo	Lo	Hi
8	Lo*	Lo	Lo	Hi*	Hi	Hi	Hi	Lo
9	Hi	Lo	Lo	Hi*	Lo*	Hi	Hi	Lo

Table 3.6 Biquinary Decode Conditions

* Denotes the actual outputs used for decode of a numeral. Decoding of the final decade is performed in a similar manner and conditions required for display of polarity and numbers are listed in Table 3.7

NUMERAL 0	IC1(6) 1	IC2(6) 2	IC3(6) +	IC1(9) $\overline{1}$	IC2(9) $\overline{2}$	IC3(9) –
0	Lo*	Lo	–	Hi	Hi*	–
1	Hi	Lo	–	Lo*	Hi*	–
2	Lo*	Hi*	–	Hi	Lo	–
+	–	–	Lo*	–	–	Hi
–	–	–	Hi	–	–	Lo*

Table 3.7 10^5 Decode Conditions

AUTO-CAL LOGIC (POSITION 2)

AUTO-CAL commands are generated, by a multivibrator, approximately once every minute, and stored until the end of any sample in progress. Upon completion of the sample, the stored command initiates the AUTO-CAL sequence; the input signal is disconnected and replaced by a positive reference source (depending upon which Plug-In Unit is being used the reference source can be a zener diode, a standard cell, or an external source), 200mS Integration Time and AUTO sample mode are selected. The Voltmeter then measures the reference in the normal manner and at the end of the sample period the input to the display counters is replaced by a 10kHz clock, which applies pulses that are counted up or down until +199 999 is totalled. An additional pulse is then applied to cause a count of +200 000. The transition from I to 2, in the most significant decade, is detected and prevents further 10kHz clock pulses from being totalled. Also, each 10kHz pulse required to correct to +200 000, controls gating circuits which apply positive or negative pulses to the positive AUTO-CAL amplifier via an isolating

transformer.
e.g. for a total of +200004, five 10kHz pulses reduce this to +199999 and generate 5 negative pulses to the positive AUTO-CAL amplifier, the next 10kHz pulse increasing the total to +200 000 and generating 1 positive pulse to the positive AUTO-CAL amplifier. Upon completion of this operation the reference source is reversed and the sequence repeated, correction being made to the negative calibration point by applying pulses to the negative AUTO-CAL amplifier.

The positive AUTO-CAL operation is then repeated to complete one AUTO-CAL sequence.

AUTO-CAL INSTRUCT

Each command is stored asynchronously by AUTO-CAL INSTRUCT bistable IC8, so that IC8(9) assumes a Lo state and IC8(6) a Hi state.

The Hi output from IC8(6):-

i) Activates IC10a (already primed by Hi output from AUTO-CAL bistable IC2(9)), which causes IC10a(5) to assume a Lo state and apply WAIT INHIBIT to WAIT bistable IC16 (control Logic, position 10).

ii) Is inverted by IC12c to apply as Lo to IC15(5) (SAMPLE bistable, Control Logic) and ensure AUTO sample mode of operation. The Lo output from IC8(9) causes IC3(9) to assume a Lo state and inhibit IC14b (Control Logic) to prevent 10kHz pulses triggering WAIT bistable IC16 (Control Logic) when WAIT INHIBIT is removed.

AUTO-CAL POSITIVE

At the end of the sample in progress, the STAT 1 bistable IC4 (Control Logic) is triggered, to give POWER STAT, but is prevented from being re-triggered by WAIT INHIBIT at IC16(10) so that the STAT 1 line, from IC4 remains Hi. The STAT 1 line Hi enables AUTO-CAL bistable IC2 to be triggered by the lagging negative edge of the first available 50Hz pulse from position 1.

IC2(6) assumes a Hi state, which:-

i) relaxes DISCONNECT relay, RLG, via the relay drive circuitry, to remove the input signal from the attenuator.

ii) energises the AUTO-CAL range relay, RLL, via the relay drive circuitry. This is a normalised range which gives a reading of 200000 ✱ for 2.039 volts of reference.

iii) energises the AUTO-CAL +ve relay RLK, via gates on position 12 already primed by the Lo output from IC4(6), to connect the reference for positive polarity.

iv) selects 200mS INTEGRATION TIME via IC10c

v) primes IC9a.

IC2(9) assumes a Lo state which:-

i) sets AUTO-CAL STAT INHIBIT bistable IC7, to inhibit the power STAT gates. IC17a and IC17b (Control Logic).

ii) inhibits gates IC4a, IC4b and IC4d (Front Panel Switching) which inhibits the 2mS, 20mS, X10 MULTIPLIER and LINE SYNC commands if selected by the front panel switches.

iii) inhibits IC10a which removes WAIT INHIBIT from IC16 (Control Logic). The positive edge of the following $\overline{50Hz}$ pulse enables IC12b (already primed by the Hi output from IC3(6)) so that IC12b(6) assumes a Lo state which initiates the first AUTO-CAL sample by triggering IC16 (Control Logic). The STAT I bistable (Control Logic) is reset by the first available MAIN CLOCK pulse the following MAIN CLOCK pulse triggering RESET bistable IC6 and READY bistable IC2. IC2(6) assumes a Hi state which applies WAIT INHIBIT to IC16 (Control Logic). The lagging negative edge of the 50Hz triggers AUTO-CAL WAIT bistable IC11 so that IC11(6) assumes a Hi state. This Hi output enables IC10d so that WAIT INHIBIT is also generated from IC10d.

At the end of the AUTO-CAL sample the READY command assumes a Lo state which triggers AUTO-CAL ±1 bistable IC4, so that IC4(6) assumes a Hi state to relax AUTO-CAL +ve relay, RLK, and energise AUTO-CAL -ve relay RLJ, thus the reference source is connected to give a negative reading for the second AUTO-CAL sample.

The STAT 1 bistable is triggered which causes the $\overline{\text{STAT 1}}$ line to assume a Lo state and trigger the single-shot circuit IC9a, IC9d, C1, C2, and R1. This sets the 10kHz NORMAL bistable IC1, so that IC1(9) assumes a Lo state and IC1(6) assumes a Hi state.

The Hi output from IC1(6):-

i) is inverted by IC10b to ensure WAIT INHIBIT is present.

ii) activates the input gate of IC19a (Control Logic) which allows 10kHz pulses to be accumulated by the display counter.

iii) activates either IC9b or IC9c (10^5 decade). If the accumulated total is greater than +200000 e.g. +200004, then IC9c is activated. If the accumulated total is less than +200000 e.g. +199996, then IC9b is activated.

iv) primes the AUTO-CAL pulse Direction Control Gates, (IC13a, IC13b, IC14a and IC14b).

The Lo output from IC1(9):-

i) inhibits AUTO-CAL bistable IC2

ii) inhibits the input AND gate of IC19a (Control Logic) to prevent entry of v-f converter pulses into the display counters.

iii) inhibits the normal count-up/count down decision gates IC9a and IC9d (10^5 Decade) so that control of COUNT UP/COUNT DOWN is fully transferred to IC9b and IC9c.

CORRECTION

AUTO-CAL POSITIVE 1

When the counter total is greater than 200000, IC9b (10^5 Decade) is inhibited by the Lo output from IC8(9) (10^5 Decade) so that IC9(6) assumes a Hi state. IC9c (10^5 Decade) is activated by the Hi output from IC8(6). so that IC9c(8) assumes a LO state. The conditions for countdown are thus satisfied. IC14a is primed by the UP command and Hi outputs from IC1(6) and IC6(9), thus, as each 10kHz pulse required to reduce the total to 199999 enters the display counters, so IC13a is enabled by the output from the 10kHz Pulse Shaper VT1, VT2 which is triggered by 10kHz pulses. Each time IC13a is enabled, the positive AUTO-CAL amplifier receives a pulse which is translated into balance voltage correction increments. As the total changes from *200000 to 199999 the outputs from IC8 (10^5 Decade) are reversed causing the UP and $\overline{UP}$ commands to become transposed which inhibits IC13a and primes IC13b. The next 10kHz pulse increases the total to +200,000 and causes the pulse shaper to activate IC13b so that a pulse is fed to the AUTO-CAL amplifier.

The change from 1 to 2 in the 10^5 decade triggers the 10kHz NORMAL bistable IC1 so that IC1(6) assumes a Lo state and IC1(9) assumes a Hi state.

The Lo output from IC1(6):-

i) inhibits IC13a, IC13b, IC14a and IC14b

ii) inhibits the gate of IC19a (control Logic) which prevents entry of further 10kHz pulses into the display counters.

iii) inhibits the AUTO-CAL COUNT-UP/COUNT-DOWN decision gates IC9b and IC9c (10^5 decade).

The Hi output from IC1 (9):-

i) removes the SET command from IC2

ii) primes the gate of IC19a (Control Logic) which permits entry of v-f converter pulses into the display counters.

10mS after the relays have switched, the negative edge of a $\overline{50Hz}$ pulse triggers AUTO-CAL WAIT bistable IC11, so that IC11(6) assumes a Lo state and inhibits IC10d so that WAIT INHIBIT is removed.

AUTO-CAL NEGATIVE

The leading positive edge of the next 50Hz pulse enables IC12b (already primed by the Hi output from IC3(6) so that IC12b(6) assumes a Lo state, which triggers WAIT bistable IC16. The second AUTO-CAL sample is initiated.

At the end of the sample, READY assumes a Lo state which triggers AUTO-CAL ±2 bistable IC6 so that IC6(6) assumes a Hi state and IC6(9) assumes a Lo state.

The Lo output from IC6(9) resets AUTO-CAL ±1 bistable, IC4, so that IC4(6) assumes a Lo state, which causes the AUTO-CAL +ve relay RLJ to be relaxed and energises AUTO-CAL -ve relay RLK. Also, IC6(9) Lo, inhibits IC6(6) IC14a and IC14b.

The $\overline{STAT\ 1}$ line assuming a Lo state triggers the single-shot circuit which initiates the change-over, of COUNT-UP/COUNT-DOWN decision, from the POLARITY bistable to the 10kHz/NORMAL and $\overline{10kHz/NORMAL}$ commands.

AUTO-CAL POSITIVE 2

The leading positive edge of the next 50Hz pulse triggers WAIT bistable IC16 (Control Logic) and initiates a second AUTO-CAL positive sample.

At the end of the sample, READY assumes a Lo state which triggers AUTO-CAL ± bistable IC6, so that IC6(6) assumes a Lo state and IC6(9) assumes a Hi state. The Lo output from IC6(6) triggers AUTO-CAL INSTRUCT bistable, IC8, so that it may accept the next AUTO-CAL INSTRUCT when generated. The Hi output from IC6(9) primes IC14a and IC1b.

When MANUAL sample is attempted during an AUTO-CAL sample, the SAMPLE STORE bistable is set so that IC5(9) assumes a Lo state and IC5(6) assumes a Hi state. At the end of AUTO-CAL, IC7(6) assuming a Lo state triggers IC5 so that IC5(9) assumes a Hi state and initiates a sample via IC9C and IC12d.

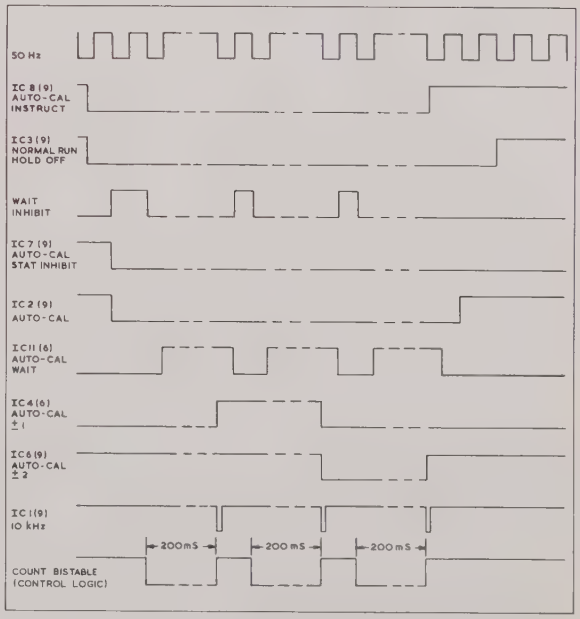


Fig.3.34 Auto-Cal Timing

TIMER COUNTER (POSITION 7)

The Timer Counter defines the duration of the Integration period during which v-f converter pulses are accumulated in the Display Counter. Three basic counting periods, 2mS, 20mS and 200mS are available and are selected by front panel switches. Each counting period can be increased by a factor of ten, to give 20mS, 200mS and 2S periods, by operation of a fourth front panel switch.
Basically, the counter comprises five divider stages and associated gates as in the block diagram of Fig. 3.35

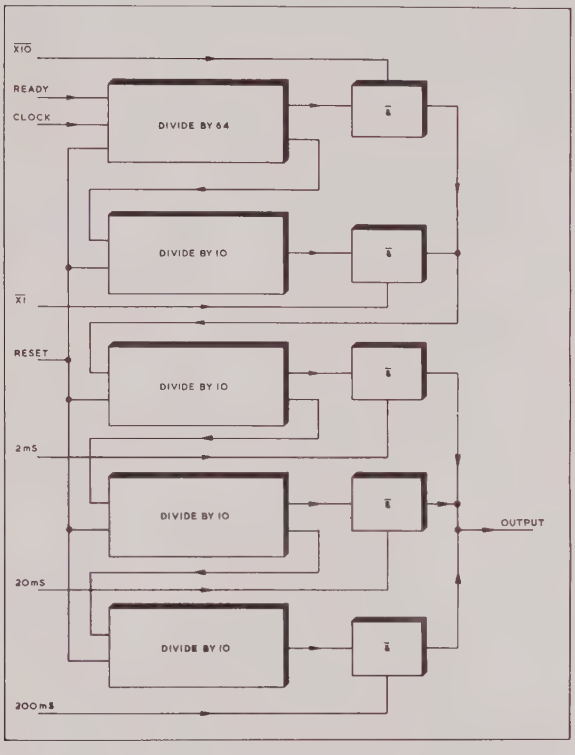


Fig.3.35 Timer Counter — Block Diagram

MAIN CLOCK pulses enter the Timer Counter at Frequency of 320kHz (50Hz Mains Supply. For 60Hz the MAIN CLOCK frequency is 384kHz), after a READY instruction, from the Control Logic, has been received. The output from the counter assumes a Lo state after:-

640	MAIN CLOCK pulses have been counted, for 2mS.
6400	MAIN CLOCK pulses have been counted, for 20mS
64000	MAIN CLOCK pulses have been counted, for 200mS
640000	MAIN CLOCK pulses have been counted, for 2S.

RESET

The Hi output from RESET bistable IC6 (Control Logic), prior to each sample is inverted by IC16a and IC16b and applied to the 'set' inputs of all bistables so that the counter is RESET to zero. Under normal operating conditions the counter resets itself, but the above ensures that the counter is reset when the integration time is changed during a measurement.

DIVIDE BY 64

MAIN CLOCK pulses trigger IC1, the first stage of a six stage 'ripple through' counter, the first pulse causing IC1(6) to assume a Hi, the second causing a Lo, which triggers IC2. An abreviated truth table for the DIVIDE BY 64 stage is shown in Table 3.8

MAIN CLOCK PULSES	IC1(6)	IC2(6)	IC3(6)	IC4(6)	IC5(6)	IC6(6)
0	Lo	Lo	Lo	Lo	Lo	Lo
1	Hi	Lo	Lo	Lo	Lo	Lo
2	Lo	Hi	Lo	Lo	Lo	Lo
3	Hi	Hi	Lo	Lo	Lo	Lo
↓						
63	Lo	Hi	Hi	Hi	Hi	Hi
64	Lo	Lo	Lo	Lo	Lo	Lo

Table 3.8 Divide by 64 Truth Table

X10 TIME MULTiplier

If the x10 facility is selected, IC15d is inhibited and the output from IC6 triggers the next DIVIDE BY TEN stage (IC11 to IC14), so that the number of pulses required to give an output is increased by a factor of ten.

DIVIDE BY TEN

The remaining stages are DIVIDE BY TEN stages, operation of each being identical. A Hi to Lo transition occurs after every ten input pulses, Table 3.9 is a truth table for the DIVIDE BY TEN stages

INPUT PULSES	IC11(6) IC7(6) IC17(6) IC22(6)	IC12(6) IC8(6) IC18(6) IC23(6)	IC13(6) IC9(6) IC19(6) IC24(6)	IC14(6) IC10(6) IC20(6) IC25(6)
0	Lo	Lo	Lo	Lo
1	Hi	Lo	Lo	Lo
2	Lo	Hi	Lo	Lo
3	Hi	Hi	Lo	Lo
4	Lo	Lo	Hi	Lo
5	Hi	Lo	Hi	Lo
6	Lo	Hi	Hi	Lo
7	Hi	Hi	Hi	Lo
8	Lo	Lo	Lo	Hi
9	Hi	Lo	Lo	Hi
10	Lo	Lo	Lo	Lo

Table 3.9 Divide by ten Truth Table

2mS INTEGRATION TIME

Selection of the 2mS count period is achieved by depression of the 2mS INTEGRATION TIME push-button switch SA1. The Lo output from IC4a (Position 13) is connected to IC15b where it is inverted to prime IC15c. The other input to IC15c is connected to IC10(9) so that every time IC10(9) assumes a Hi state, the AUXiliary output from the Timer Counter assumes a Lo.

20mS INTEGRATION TIME

Selection of the 20mS count period is achieved by depression of the 20mS INTEGRATION TIME push-button switch SA.2. The Lo output from IC4a (Position 13) is connected to IC21a where it is inverted to prime IC21d. The other input to IC21d is connected to IC20(d) so that every time IC20(9) assumes a Hi state, the AUXiliary output from the Timer Counter assumes a Lo.

200mS INTEGRATION TIME

Selection of the 200mS count period is achieved by depression of the 200mS INTEGRATION TIME push-button switch SA3. The Lo output from IC4a is connected to IC21b where it is inverted to prime IC21c. The other input to IC21c is connected to IC25(9) so that every time IC25(9) assumes a Hi state, the AUXiliary output from the Timer Counter assumes a Lo.

AUTO RANGE (POSITION 5)

By setting the Range Selector Switch, on the front panel, to AUTO RANGE 200V MAXimum, the voltmeter automatically selects the range which gives optimum resolution. Fig. 3.36 is a block diagram of the AUTO-RANGE board which includes the REMOTE RANGE command inputs.

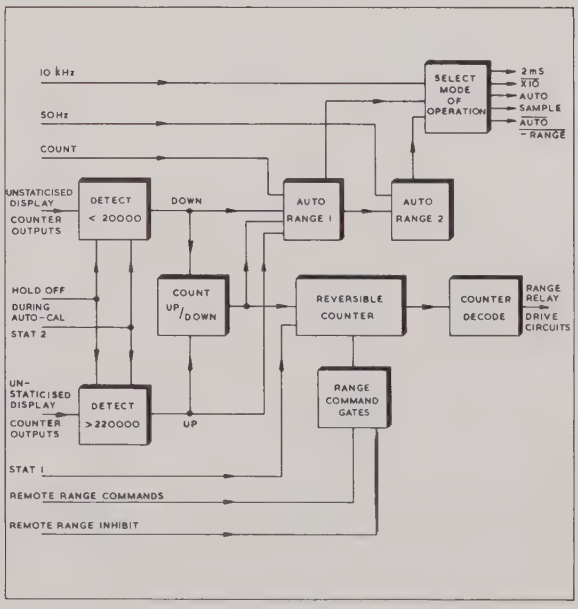


Fig.3.36 Auto-Range

Unstaticised outputs from the display counters control a COUNT UP/COUNT DOWN decision, which is made when the count exceeds 220000 or falls below 20000. If either of these conditions is detected AUTO-RANGE 1 is triggered by the end of count signal, so that 2mS INTEGRATION TIME and AUTO are selected, and the power stat gates are inhibited to prevent the available result of measurement from being displayed.

The first MAIN CLOCK triggers STAT 1 (Control Logic) which in turn triggers the reversible counter to select the next range. The negative edge of the next 50Hz pulse triggers AUTO-RANGE 2 which primes a gate so that the lagging positive edge of the same pulse can initiate a measurement on the new range.

If at the end of this measurement further ranging is required the counter is stepped so that the next range is selected and a new measurement is initiated by the negative edge of a 50Hz pulse. This is repeated until a suitable range is found.

When this occurs the end of count signal resets AUTO-RANGE 1 so that operation is controlled by either the front panel controls or the rear socket commands. A 10kHz pulse initiates measurement with the correct range selected and under the programmed conditions.

The use of the 50Hz pulses to initiate AUTO-RANGE measurements enables the instrument to settle after range changes.

AUTO RANGE

Selection of AUTO RANGE removes AUTO RANGE INHIBIT which activates IC16a (provided that AUTO-CAL is not in progress), and primes the counter decode gates IC12a, IC11a, IC11c, IC11b and IC12b. Depending upon the state of the counter one of the ranges will be selected. The SET input to AUTO RANGE 1 bistable is removed by the Hi output from IC16b and IC16d.

DOWN RANGING

Down ranging occurs only when the following conditions are satisfied:-

i) The outputs from $\overline{2_5}$, $\overline{1_5}$, $\overline{8_4}$, $\overline{4_4}$ and $\overline{2_4}$, stages are Hi (which only occurs when the total number pulses accumulated by the display counter is equal to or less than 19999).

ii) AUTO RANGE HOLD OFF is Hi.

iii) STAT 2 is Hi (this ensures that neither DOWN-RANGE nor UP-RANGE decisions are taken until the end of the second sample, when LINE SYNC is selected).

iv) The output from IC3b is Hi (IC3b is a 'detect zero' gate from the reversible counter. When zero is detected the output assumes a Lo state which inhibits IC1a, preventing further DOWN-RANGE commands).

When the previous conditions are satisfied, IC1a(6) assumes a Lo state. The Lo output from IC1a inhibits IC15a, IC13a, IC13b, and IC10c. IC15a output assumes a Hi state which primes IC15b.
At the end of the sample, the COUNT line assumes a Lo state which triggers AUTO-RANGE 1 bistable IC7 so that IC7(6) assumes a Hi state and IC7(9) assumes a Lo state.
The Hi output from IC7(6):-

i) primes IC8c

ii) is inverted by IC17b so that IC14b and IC17a (Control Logic) are inhibited thus preventing triggering of WAIT bistable IC16 (Control Logic) by 10kHz pulses and inhibiting POWER STAT.

iii) is inverted by IC17a so that 2mS integration time is selected.

iv) is inverted by IC17c so that x10 TIME MULTiplier is inhibited.

v) is inverted by IC16c so that the SAMPLE line is held Lo for AUTO sample operation.

The Lo output from IC7(9) inhibits IC8b and inhibits the programmed integration time.

The first available MAIN CLOCK pulse to occur after the end of COUNT triggers STAT 1 bistable IC4 (control logic) so that STAT 1 assumes a Hi state which triggers the single shot circuit IC15d, IC15c, C1 and C2 via IC15b.
4μS later the output from IC15d assumes a Lo state which synchronously triggers the stages IC4, IC5 and IC6 of the reversible counter so that it counts down by one bit. This causes the counter decode gates IC12a, IC11a, IC11c, IC11b and IC12b to select the next range down e.g. 2V in place of 20V.

The first available negative edge of a 50Hz pulse to occur after the triggering of AUTO RANGE 1 bistable IC7, triggers AUTO RANGE 2 bistable IC9 so that IC9(6) assumes a Hi state. This Hi output primes IC8c and is also inverted by IC17d to ensure that $\overline{\text{AUTO RANGE}}$, to the Control Logic, is maintained after IC7 has been re-triggered. The lagging positive edge of the same 50Hz pulse initiates a 2mS sample on the new range.

If at the end of the sample, the voltmeter does not require further downranging, IC1a output assumes a Hi state which activates IC15a (already primed by the Hi output from IC2a and IC2b) which in turn inhibits IC15b preventing the counter from being triggered. The COUNT line going Lo triggers AUTO-RANGE 1 bistable IC7 so that IC7 (6) assumes a Lo state and IC7(9) assumes a Hi state.

The Lo output from IC7(6):-

i) inhibits IC8c

ii) is inverted by IC17a to inhibit the 2ms integration time

iii) is inverted by IC17c to release the x10 function

iv) is inverted by IC16c to that the mode of operation i.e.

AUTO/MANUAL is controlled by either the rear socket commands or the front panel switches.
The Hi output from IC7(9):-

i) primes IC8a

ii) returns the control of INTEGRATION TIME to the rear socket commands or the front panel switches.

iii) primes IC8b (in conjunction with the Hi output from IC9(6)). The first available 10kHz pulse activates IC8b and initiates a sample under the programmed conditions. The COUNT line assumes a Hi state which enables IC8a so that IC9 is reset.

UP RANGING

Upranging only occurs when the following conditions are satisfied:-

i) The outputs from the 2_5 and either the 2_4 or 4_4 stages are Hi (which occurs when the total number of pulses accumulated by the display counter is equal to or greater than 220000).

ii) STAT 2 is Hi

iii) The output from IC6(9) is Hi (indicating that the 200V Range is not being used).

iv) AUTO RANGE HOLD OFF is Hi.

Whenever the previous conditions occur, the junction at IC2a(6) and IC2b(8) assumes a Lo state. The Lo output from IC2 inhibits IC15a, IC1b, IC3c, IC3a and IC10b. IC15a output assumes a Hi state which primes IC15b.

At the end of the sample the procedure is the same as for down ranging with the exception that the reversible counter is gated so that it counts up by one bit. The counter decode gates select the next range up e.g. 20V in place of 2V.

REMOTE RANGING

When the REMOTE RANGE function is selected by the front range switch REMOTE RANGE INHIBIT assumes a Hi state which is inverted by IC16b to inhibit operation of AUTO RANGE 1 bistable IC7 and primes the REMOTE RANGE COMMAND gates IC13c, IC13d, IC14b, IC14d and IC14c

The outputs from these gates are applied to SET and RESET inputs at each of the counter stages and thus conditions the counter which controls the range selector gates.

The commands are presented to the rear socket in 124 BCD form and Table 3.10 lists the ranges selected by each command.

RANGE	COMMAND INPUT		
	SKAm(1)	SKAn(2)	SKAp(4)
20mV	Lo	Lo	Lo
200mV	Hi	Lo	Lo
2V	Lo	Hi	Lo
20V	Hi	Hi	Lo
200V	Lo	Lo	Hi

Table 3.10 Range Commands

RELAY DRIVE BOARD (POSITION 12)

The relay drive board contains the decode and drive circuits for the input attenuator relay, the range relays and the AUTO-CAL relays. Range commands are derived either from SC.1F or the counter decode gates of the AUTO-RANGE board.

20mV Range

When the 20mV range is commanded pin 22, of the input connector, assumes a Lo state which, inverted by IC2d, causes VT4 to conduct and energise RLC. The same Lo inhibits IC1a so that the Hi output causes VT2 to conduct and energise RLB. Also, during normal operation i.e. the voltmeter is not performing AUTO-CAL, pin 2 is Lo which, inverted by IC6d, causes VT9 to conduct and energise RLG.

200mV Range

When the 200mV range is commanded pin 23 assumes a Lo which inverted by IC3d, causes VT5 to conduct and energise RLD. The same Lo inhibits IC1a so that the Hi output causes VT2 to conduct and energise RLB. Also, during normal operation, pin 2 is Lo which, inverted by IC6d, causes VT9 to conduct and energise RLG.

2V Range

When the 2V range is commanded pin 20 assumes a Lo which inhibits IC3c and causes VT6 to conduct and energise RLE. The same Lo inhibits IC1a so that the Hi output causes VT2 to conduct and energise RLB. Also, during normal operation pin 2 is Lo which, inverted by IC6d, causes VT9 to conduct and energise. RLG

20V Range

When the 20V range is commanded, pin 24 is Lo which inhibits IC5a and causes VT8 to conduct and energise RLF. The same Lo inhibits IC1a so that the Hi output causes VT2 to conduct and energise RLB. Also, during normal operation, pin 2 is Lo which, inverted by IC6d, causes VT9 to conduct and energise RLG.

200V Range

When the 200V range is commanded pin 18 assumes a Lo which inhibits IC3c and IC2b and causes VT1 and VT6 to conduct and energise RLA and RLE (2V range and 100 to 1 attenuator) respectively. All inputs to IC1a are Hi so that IC1a(6) assumes a Lo and cuts off VT2 which relaxes RLB. During normal operation pin 2 is Lo which, inverted by IC6d, causes VT9 to conduct and energise RLG.

1000V Range

When the 1000V Range is commanded pin 19 is Lo which inhibits IC5a and IC2b causing VT1 and VT8 to conduct and energise RLA and RLF (20V range and 100 to 1 attenuator) respectively. All inputs to IC1a are Hi so that IC1a(6) assumes a Lo and cuts off VT2 which relaxes RLB. During normal operation, pin 2 is Lo which, inverted by IC6d causes VT9 to conduct and energise RLG.

RANGE INDICATION

IC3a, IC3b and IC1b translate the range commands into 124 BCD form so that range identification may be effected via the rear socket (SKA).

Table 3.11 lists the operating conditions of this circuit

RANGE NO.	RANGE	IC3b(4)	IC3b(5)	IC3a(1)	IC3a(2)	IC1b(13)	(1) IC1b(8)	(2) IC3a(3)	(4) IC3b(6)
0	20mV	Hi	Hi	Hi	Hi	Hi	Lo	Lo	Lo
1	200mV	Hi	Hi	Hi	Hi	Lo	Hi	Lo	Lo
2	2V	Hi	Hi	Hi	Lo	Hi	Lo	Hi	Lo
3	20V	Hi	Hi	Lo	Hi	Hi	Hi	Hi	Lo
4	200V	Hi	Lo	Hi	Hi	Hi	Lo	Lo	Hi
5	1000V	Lo	Hi	Hi	Hi	Hi	Hi	Lo	Hi

Table 3.11 Range Identification

AUTO-CAL

During AUTO-CAL IC2(6) (AUTO-CAL LOGIC) assumes a Hi state which:-

i) is inverted by IC4a to cut off VT4, VT5, VT6 and VT8 and relax the range relays.

ii) is inverted by IC6(d), (so that RLG is relaxed), and again by IC6c so that RLL is energised.

iii) primes IC6a and IC5d.

AUTO-CAL ± is initially Lo which inhibits IC6a and, after inversion by IC5b, activates IC5d. The Lo output from IC5d inhibits IC5c so that VT12 conducts and energises RLK.

When AUTO-CAL ± assumes a Hi state IC6a is activated and IC5d inhibited. The Lo output from IC6a inhibits IC6b so that VT11 conducts and energises RLJ.

AUTO-CAL ± returns to a Lo and RLK is energised again. At the end of AUTO-CAL, IC2(6) (AUTO-CAL Logic) assumes a Lo which inhibits both IC6a and IC5d and after inversion by IC4a, reverse biases MR7, MR9, MR11 and MR14 so that range control is restored.

FRONT PANEL SWITCHING

AUTO SB1: The AUTO push button connects 0V to the SAMPLE bistable (Control Logic) which sets it to the continuous sample state.

MANUAL. SB2: Depression of the MANUAL button releases the AUTO button and causes a negative going pulse at pin 30 board 13. This pulse sets the SAMPLE bistable (Control Logic) which is reset at the end of the measurement.

2mS SA1: Depression of SA1 disconnects 250V from the displays of the last two decades and, providing that AUTO-CAL and AUTO-RANGE are not in progress, primes the 2mS count period gate (Timer Counter).

20mS SA2: Depression of SA2 disconnects 250V from the last decade and, providing that AUTO-CAL and AUTO-RANGE are not in progress, primes the 20mS count period gate.

200mS SA3: Depression of SA3 primes the 200mS count period gate only when AUTO-CAL and AUTO-RANGE are not in progress.

x10 SA4: With SA4 'out' and when AUTO-CAL and AUTO-RANGE are not in progress IC4b output (Lo) primes the x1 count period gate.
With SA4 'in' and with the same restrictions IC4b output primes the x10 count period gate.

LINE SYNC SA5: When depressed, and provided that AUTO-RANGE and AUTO-CAL are not in progress, SA5 enables the output from IC4d to inhibit IC14b (Control Logic) and IC19b (10) (Control Logic) and prime the LINE SYNC gates, IC13a and IC13b (control logic).

CAL SA7: When SA7 is 'out' and the AUTO CAL COMMAND switch (SE) is in the 'INTernal' position, the AUTO-CAL gates on the Relay Drive Board are primed by commands from the AUTO-CAL bistable IC2 (Position 2) via SA7. Also externally applied AUTO-CAL commands at SKA/g set the AUTO-CAL INSTRUCT bistable IC8 (Position 2).

Depressing the CHECK CAL switch (SA7) produces a negative pulse which 'sets' the AUTO-CAL INSTRUCT bistable. MR11 prevents the pulse from rising above +5V when the switch is released.

FILTER SA6: When SA6 is depressed RLH is energised and a 100mS single section filter connected at the input.

DECIMAL POINT DRIVE

The decimal point drive is derived from the range commands via the decoding network IC1a, IC2, IC3 and IC4c. When decimal point setting is determined by the sub-unit, the decode network is inhibited by switching to SUB-UNIT on the range switch, and the commands from the sub-unit applied to IC2c, IC2b IC3c and IC4c.

***ILP.5:** ILP5 is illuminated either when a count exceeds 220000, as detected by IC1d and IC1c or during AUTO-CAL as indicated by $\overline{\text{AUTO-CAL}}$ assuming a Lo condition. In both cases VT1 is cut-off so that ILP5 strikes.

mV and V: IC6b and IC6a monitor the range commands to determine which units, mV or V, are to be displayed. When IC6b output assumes a Hi (either 2V, 20V, 200V or 1000V range commanded) IC5d is activated and IC5c inhibited so that VT6 conducts and causes ILP7 to strike. When IC6a output assumes a Hi (either 20mV or 200mV range commanded) IC5a is activated and IC5b inhibited so that VT7 conducts and ILP6 strikes.

If SUB-UNIT is selected on the range switch, automatic units selection is inhibited by 0V to IC5d and IC5a, and the command applied to IC5c and IC5b.

$\overline{\text{AUTO-CAL}}$ and $\overline{\text{AUTO-RANGE}}$

These commands are normally Hi so that IC's 4a, 4b and 4d are activated and control of integration is by the push button switches. When either of the commands assumes a Lo IC's 4a, 4b and 4d are inhibited and control of integration is by the AUTO-RANGE or AUTO-CAL logic.

FLUX OSCILLATOR (POSITION 16)

When the voltmeter is switched on the appearance of the +40V rail causes VT1 to conduct which in turn causes VT3 to conduct and VT4 to cut off. Pin 2 goes positive and the primary of T1 (Floating Power Supply) draws current through R7 at a rate determined by T1 primary inductance. Pin 6 goes positive and maintains VT1 (and hence VT3) in conduction.

When T1 core has saturated and the rate of change of flux, in T1 core, is zero pin 6 goes negative causing VT1 to cut off and VT2 to conduct. VT3 cuts off and VT4 conducts produce an identical rate of change of current through T1 primary as before but in the opposite direction. Hence VT2 and VT4 are held in conduction until T1 saturates again. Thus T1 primary is switched between 0V and +40V.

FLOATING POWER SUPPLY (POSITION 18)

All supplies to the floating circuits are derived from SEC 1 of the Flux Oscillator transformer T1.

±18V Supplies
These supplies comprise two full wave rectifiers, MR1 and MR2 for positive and MR3 and MR4 for negative and two filters C4, R4, C5 and C3, R5, C6.

±36V Supplies
These supplies comprise two voltage doublers C10 MR8, MR7 and C8 (+36V) and C11, MR9, MR10 and C7 (-36V).

Buffer Amplifier Chopper Drive
The chopper drive to the buffer amplifier (Position 20) is derived directly from SEC.2.

Buffer Amplifier Demod. Drive
The demodulator drive to the buffer amplifier (Position 20) is derived from a potential divider (R2, R3).

POWER SUPPLY (POSITION 1)

Three regulated supplies provide +40V, +5V and +13V. Operation of each supply is similar and a block diagram of the basic arrangement is shown in Fig. 3.37

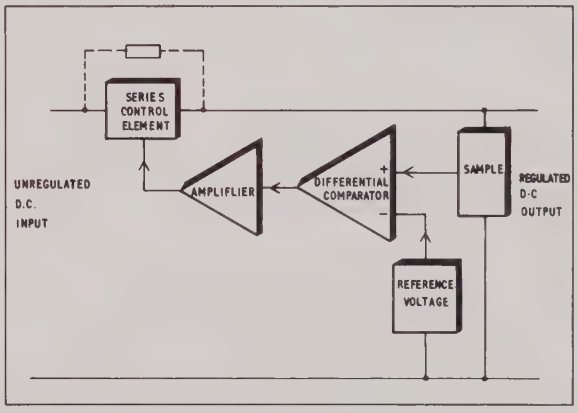


Fig.3.37 Power Supply — Block Diagram

The output voltage is sampled via a resistive chain and this sample compared with a reference voltage. The difference between the sample and the reference is amplified and controls conduction of the series element so as to regulate the load.

Each of the supplies is dependant upon the other two during operation, therefore, resistors R1, R2 and R4 by-pass the series elements of the 40V and 5V to provide initially unregulated supplies which enable the 13V supply. They also provide a bleed by for the series elements, thus minimising the dissipation in these elements.

Two full wave rectifiers provide +250V, +75V (via R6 and R7) and 12V supplies for the display tubes and the Fan Out Units respectively.

AUTO-CAL TIMER

The AUTO-CAL timer is a free running, cross coupled multivibrator. R25 and C3 define a time constant of approximately two minutes whilst R26 and C2 define a time constant of approximately 10mS, thus the output from VT13 collector is a positive pulse of 10mS duration every 2 minutes. This pulse is inverted by VT14 and stored asynchronously by the AUTO-CAL INSTRUCT bistable.

10kHz Generator

The 10kHz Generator is a cross coupled multivibrator which is turned off when STAT 1 is Lo i.e. during counting, by forward biasing MR18 which holds VT15 off'

50Hz Generator

Antiphase 50Hz applied to pins 14 and 15 is clipped to 0 and +5V by MR12 – MR15 and inverted by IC1d and IC1f.

The resultant antiphase square waves trigger the flip-flop comprising IC1e and IC1a. IC1b inverts the flip-flop output to give $\overline{50Hz}$ which is re-inverted to give 50Hz.

POSITIVE LOGIC FAN OUT UNIT EX1488

The unit comprises of two printed circuit boards which provide buffer stages between the voltmeter and the system in which it is to be used. Wire link programming provides a choice of either +5V or +12V operation. Other facilities selected by wire link.

Programming are:

i) positive or negative level Print Command.

ii) positive or negative pulse Print Command.

iii) Contact Sample noise immunity

iv) fixed characters (decimal 12) in place of the least significant or two least significant decades of display information.

POSITION 14

The Fan Out board of position 14 contains the buffer stages of the 10^5, 10^4 and 10^3 decades (including polarity) and the Print Command circuitry.

Each of the display buffers comprises an I.C. inverter followed by a common emitter stage with a 1.5kΩ load capable of sinking a further 10mA. A Hi at the input of an inverter, which signifies that a bit has been stored, results in a Lo at the output of the inverter which cuts off the following common emitter stage to produce a 1(+5V or +12V) output. Similarly, a Lo at the input results in a 0 (0V) output.

PRINT COMMAND (LEVEL)

The Print Command level at SKA/v is derived from Power Stat. With pins 4 and 5 linked Print Command Level is the inverse of Power Stat. and remains at a 0 for the duration of the measurement after which it goes to 1 (+5V or +12V).

With pins 4 and 6 linked the Print Command Level is identical to Power Stat.

PRINT COMMAND (PULSE\

Positive: With pins 9 and 8, and 10 and 11 linked VT15 is conducting, and is cut off by a negative pulse to produce a positive pulse at SKA/μ. The negative pulse is produced by C1 and R21 differentiating the Print Command Level at VT14 collector. Although both positive and negative pulses appear at the base of VT15, the positive pulse has no affect because VT15 is already conducting.

Negative: With pins 7 and 8, and 12 and 13 linked VT15 is cut off, and is turned on by a positive pulse from the differentiated Print Command Level at VT13 collector.

POSITION 15

The Fan Out board of position 15 contains the Buffer stages of the 10^2, 10^1, and 10^0 decades and the Contact and Pulse Sample circuitry.

Operation of the display buffers is identical to those on position 14.

When pins 7, 8 and 9, 10 and 11, and 12 and 13 are linked, the outputs from SKA pins D,C,B, and A are 1, 1, 0 and 0 respectively. Similarly when pins 14, 15 and 16, 17 and 18, and 19 and 20 are linked, the outputs from SKA pins J.H.F and E are 1, 1, 0 and 0 respectively.

CONTACT SAMPLE

When SKA/s is connected to 0V (SKA/HH) VT13 is cut off causing VT15 to conduct. The resulting Lo at pin 8 'sets' the SAMPLE bistable of position 10 via C1 on position 13.

To prevent contact bounce or noise from initiating an unwanted reading pins 4, 5 and 6 can be linked to provide a high degree of noise immunity.

PULSE SAMPLE

When a positive pulse of amplitude +12V or +5V and duration greater than 10μS, is applied to SKA/t VT14 emitter goes positive causing VT15 to conduct. The SAMPLE bistable of position 10 is 'set' via C1 of position 13.

SECTION 4 SERVICING

Introduction

The following information is included to assist in the location and rectification of faults, and replacment of defective items.

Recommended Tools

Large and small 'Pozidriv' screwdrivers
Screwdriver with ¼" flat blade
Screwdriver with 1/8" flat blade
Box Spanner ¼"W (5/16" BSF)
Set of open-ended B—A spanners (even sizes)
Pair of tweezers or long nosed pliers
The above tools will enable all the servicing, described in the following paragraphs, to be carried out. Additionally, where components are to be removed it will be necessary to use a soldering iron in conjunction with a solder pump to remove excess solder.

DISMANTLING INSTRUCTIONS

Before attempting to dismantle the LM1490, disconnect the instrument from the mains a.c. supply.

Removal from Case

Using the large 'Pozidriv' screwdriver, remove the four screws from the bottom edge of the front panels (LM1490 and Sub-Unit). Push the voltmeter rear panel until the instrument projects far enough from the case to be gripped The instrument and sub-unit can now be withdrawn from the case.

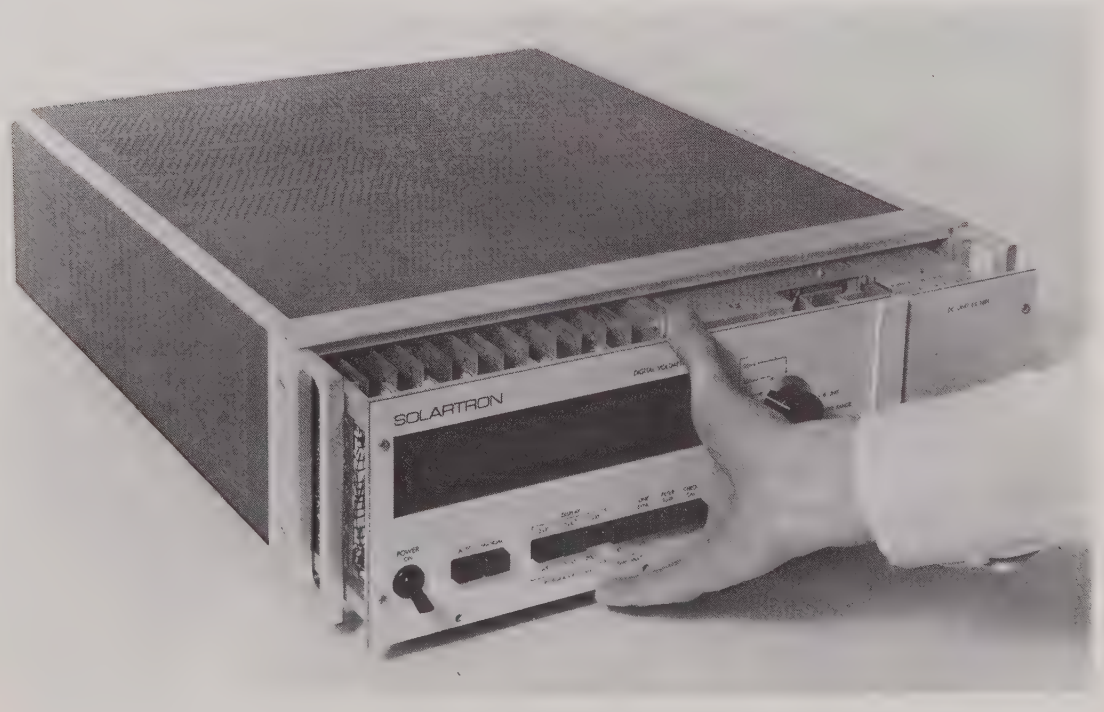


Fig. 4.1 Removal from Case

Apply slight pressure to the rear of the sub-unit, just below the rear input connector, so that the connecting plugs and sockets are disengaged. The sub-unit can now be withdrawn by gripping the rear of the screening box and pulling from the front.

Note: The sub-unit must be removed before the earthed and floating sections can be separated.

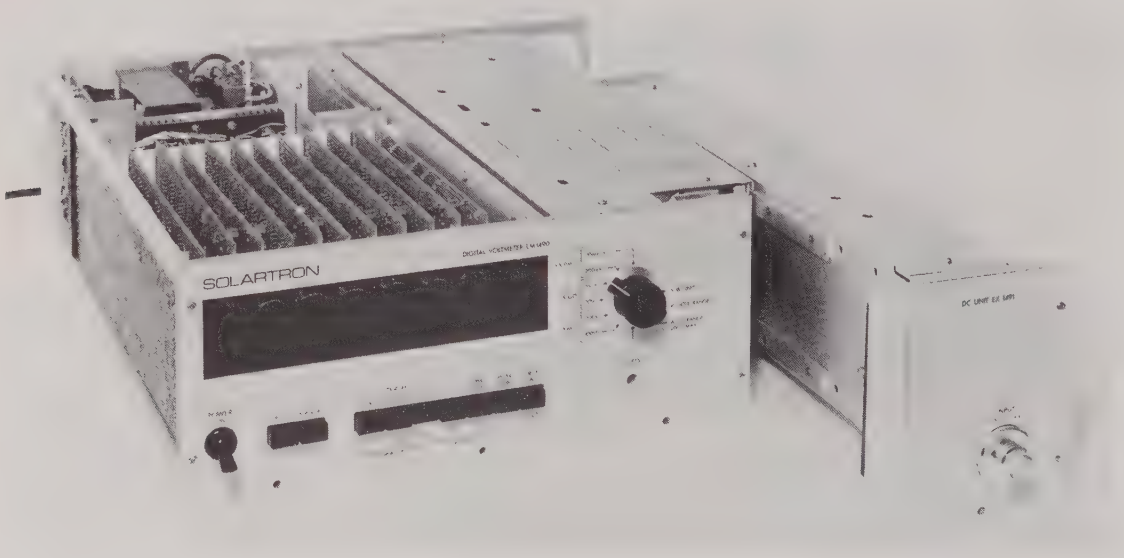


Fig. 4.2 Removal of Sub-unit

Earthed Section Board Location

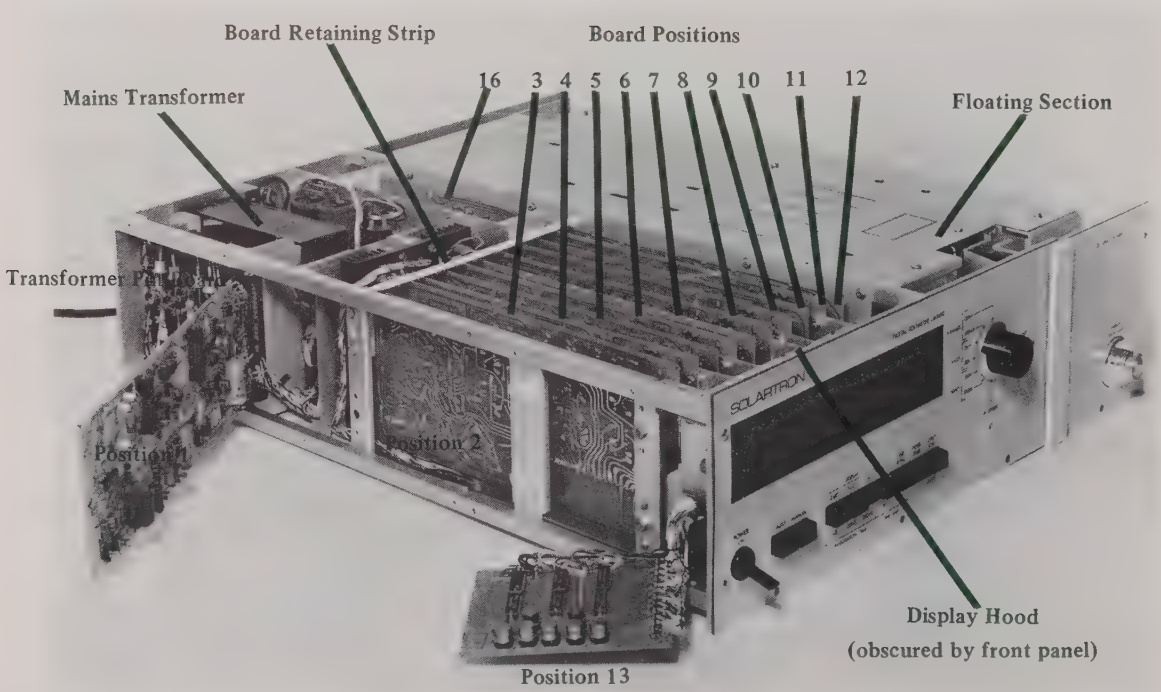


Fig. 4.3 Board Location-Earthed Section

Access to Positions 1 and 13

Position 1: The power supply board is fitted to the left side of the chassis and is hinged near the mains transformer. To swing the board out, remove the two screws which secure the board at the forward end, and apply outward pressure to the board.

Position 13: The decimal point drive board is fitted to the left side of the chassis, forward of the power supply board, and hinged on its own cable form. To swing the board out, remove the four screws which secure the board and apply outward pressure to the board.

Board Removal from Positions 2 to 12

Caution: Boards must not be removed or replaced while the instrument is switched on.

Remove the board retaining strip which is secured by three screws.

Positions 5, 7 and 12: Grip the board to be removed at each end and ease it from its location.

Positions 2 and 10: Both these boards have additional wiring attached by means of 'disconnect' pins. Thus, the method of removal is to grip the board at each end and ease the board from its location until the 'disconnects' are exposed, remove the 'disconnects' with tweezers or pliers and remove the board.

Positions 3, 4, 6, 8, 9 and 11: Before any of the display boards can be removed the display hood must be removed. To do this, remove the two 'Posidriv' securing screws and prise off the hood with a flat blade screwdriver. The boards can be removed by gripping at each end and easing from their location.

Board Removal from Positions 14, 15 and 16

First remove the short board retaining strip by slackening the two retaining screws and lifting the strip. The boards can be removed by gripping at each end and easing from the location.

Access to Boards of Floating Section

Of the boards in the floating section those in positions 18, 20, 21, 22 and 23 only are removable without first separating the earthed and floating sections (i.e. not board 17).

Board Removal from Positions 18 to 23

First remove the top cover of the screening box. This is achieved by removing the three securing screws (2 front, 1 rear) and lifting the top cover until the left hand side clears the relays of position 17.

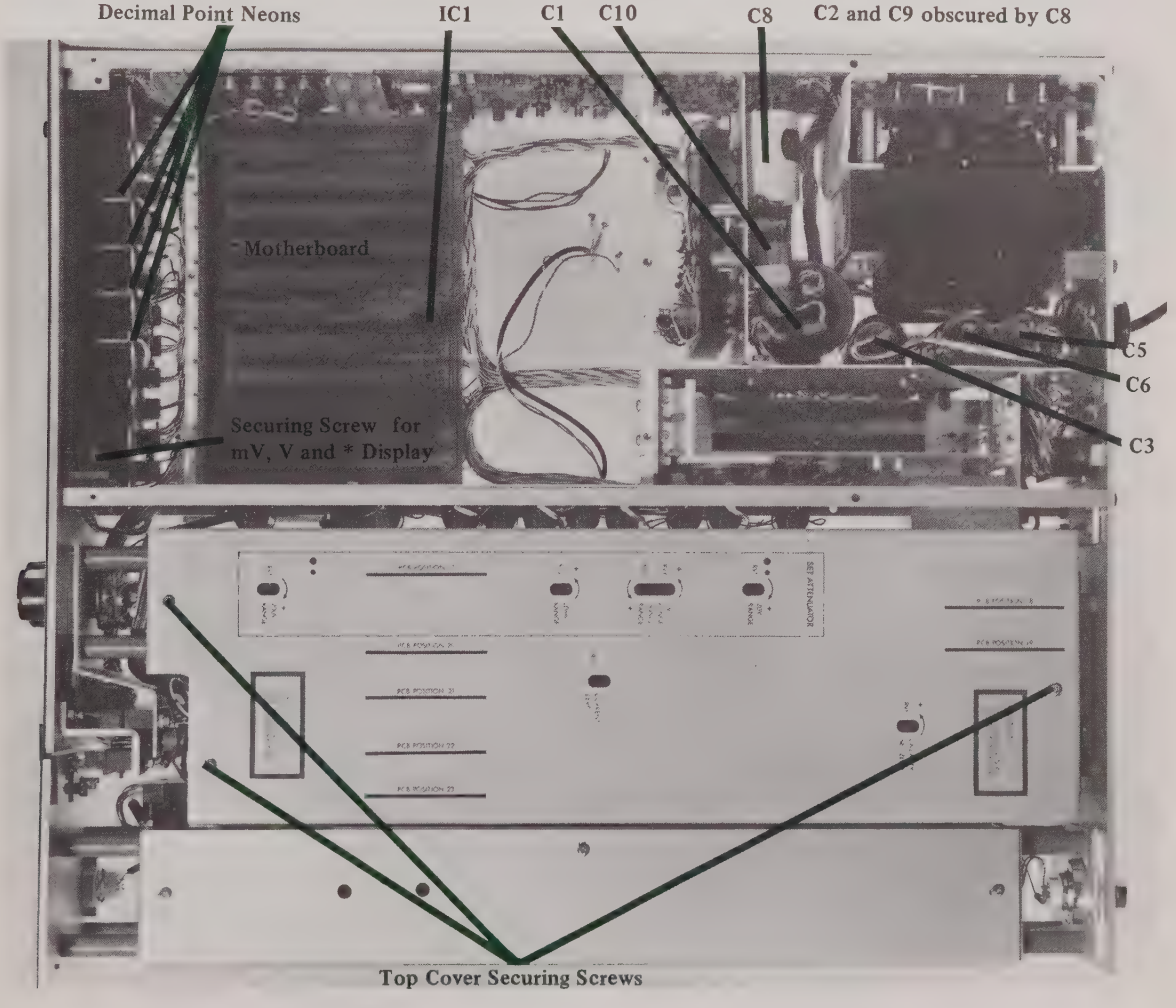


Fig. 4.4 Plan of LM1490 with Earthed Section Boards Removed

Position 18: The floating power supply can be removed by easing the board from its edge connector and raising it until the three 'disconnects' of the connecting cable are sufficiently exposed to permit disconnection.

Position 20 and 21: The buffer and input amplifiers can be removed by easing from their locations.

Positions 22 and 23: Both boards can be removed by easing from their edge connectors after first removing the 'disconnects' (4 on each board).

Separating the Earthed and Floating Sections

The sub-unit must first be removed before separation is possible. Remove the insert from the range selector knob to expose the collet securing nut which can be slackened using the ¼"w box spanner. Remove the knob. Remove the two rear screws (Fig. 4.5) which secure the two sections. The isolated (floating) and earth sections can be separated by pulling the floating section back (from rear) until the plugs and sockets are disengaged.

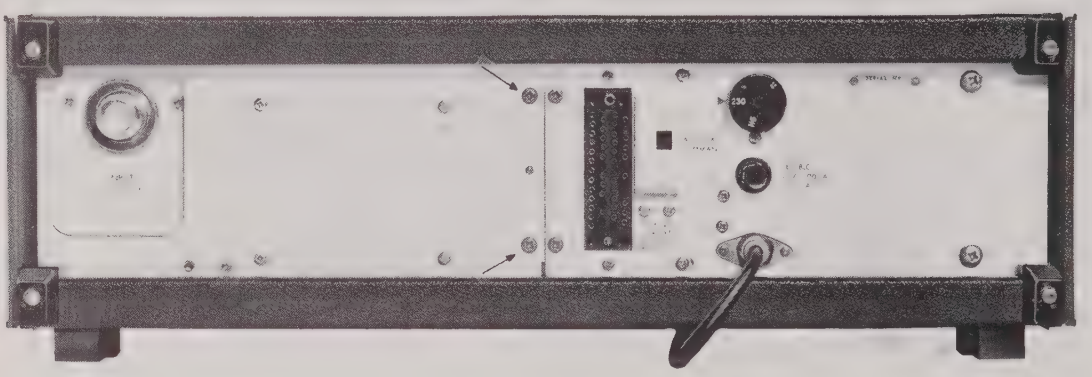


Fig. 4.5 Rear View

Caution: The two sections are still connected at the rear by the cable which connects the flux oscillator to the floating power supply. This cable is attached by means of four 'disconnect' terminals on the motherboard of positions 14, 15 and 16.

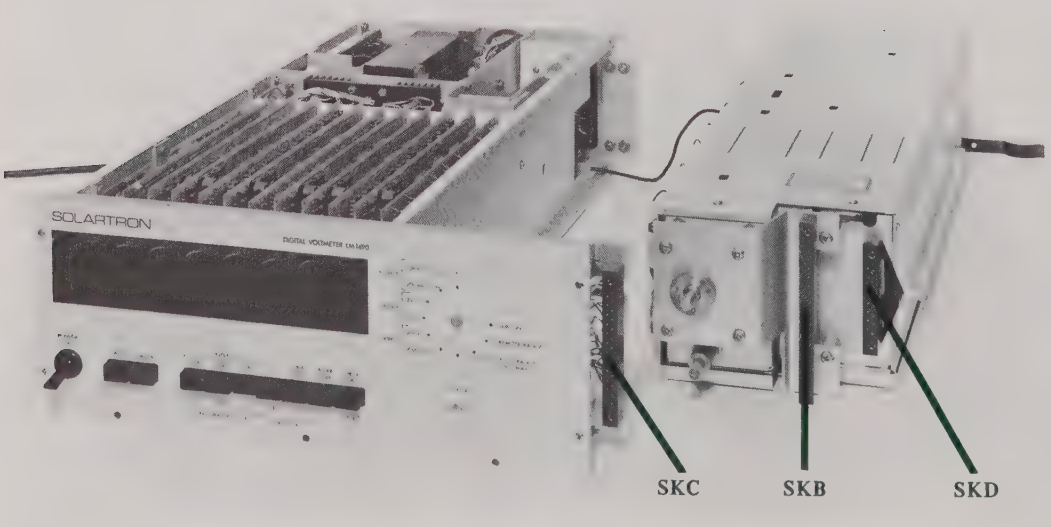


Fig. 4.6 Earthed and Floating Sections-Separated

Position 17: The input switching board is not removable, but, after easing the board out of its location, it can be hinged on its cableform.

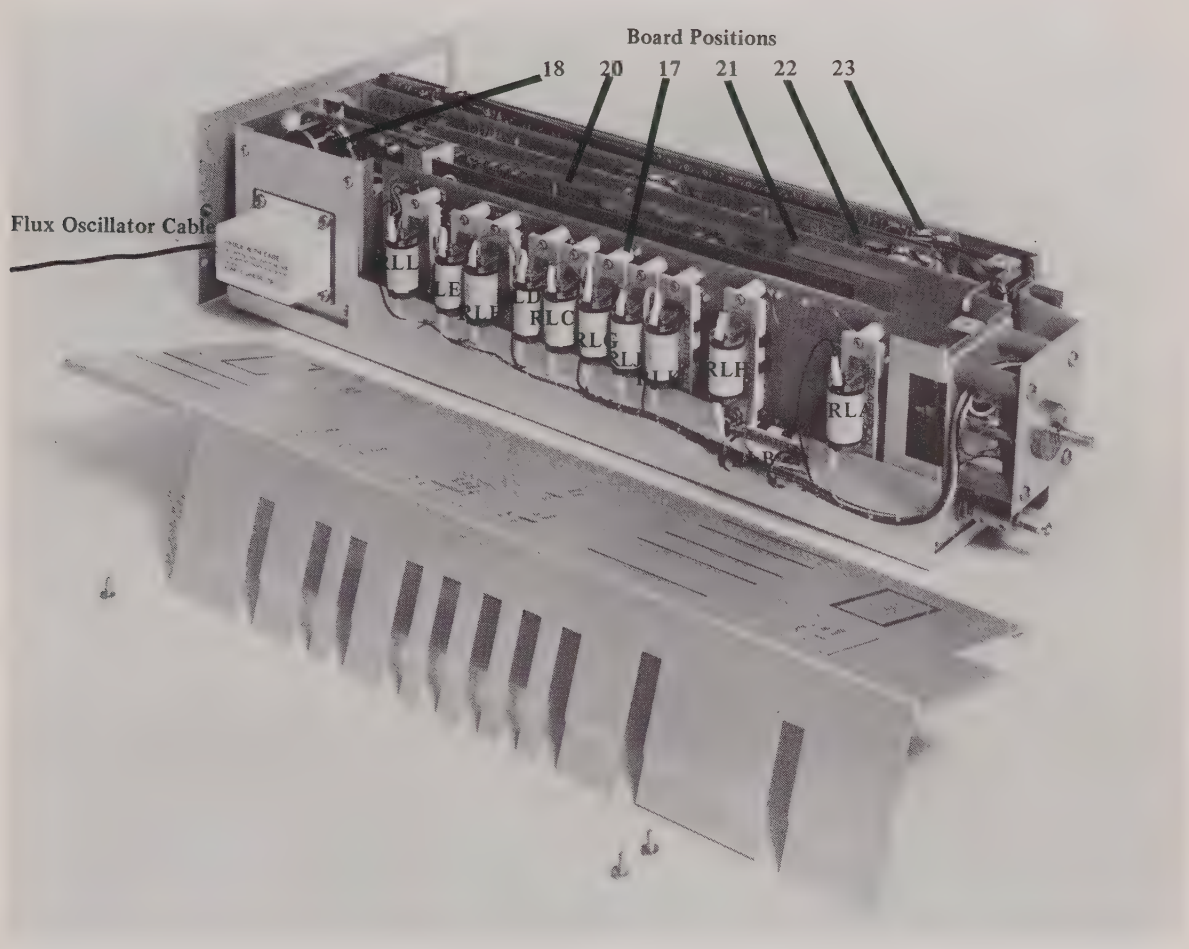


Fig. 4.7 Floating Section

Input Switching Relays mV, V,* Display

Once the instrument has been separated it is possible to remove the mV, V, * display by undoing the display securing screw (Fig. 4.4) and unsoldering the six connections.

The coils of the input switching relays can be removed after the two securing screws have been removed and the two connections unsoldered. Board 17 must be raised to expose the lower securing screw.

Access to wiring of Floating Unit.

The wiring of the floating unit is situated under the bottom cover of the screening box which can be removed after undoing four securing screws.

Access to Push Button Switches

All connections are accessible immediately behind the front panel, when the chassis is inverted.

Replacement of Decimal Point Neons

Remove all the boards in positions 2 to 12, unsolder the two connections of the appropriate neon and extract with a direct pull.

Access to Sub-Unit Boards

Remove the Sub-Unit screening box cover which is secured by five screws (3 on top, 2 on right hand side).

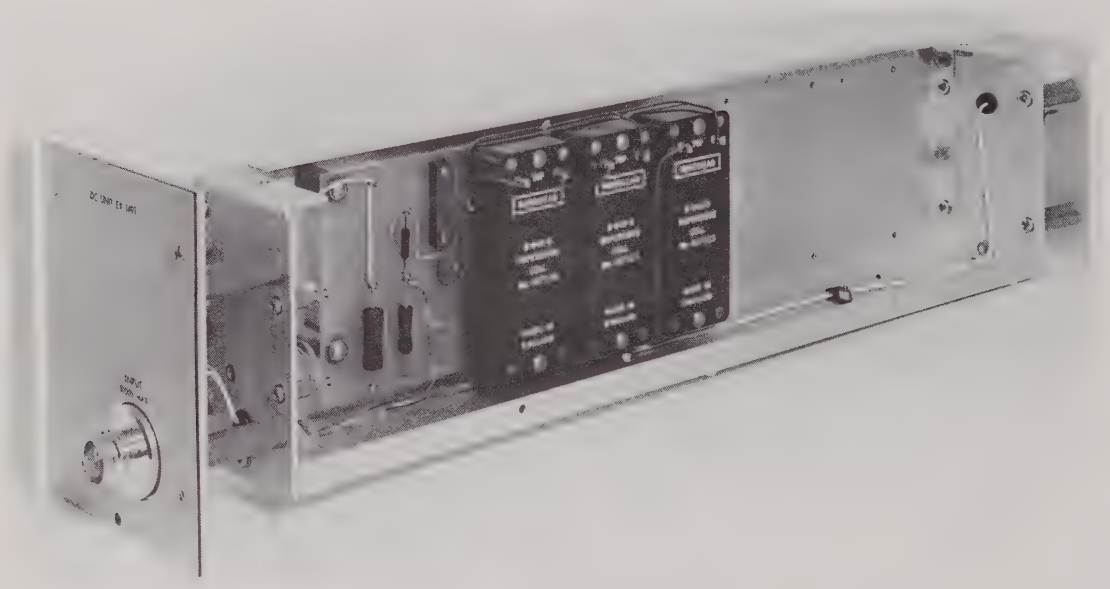


Fig.4.8 DC Unit EX1491

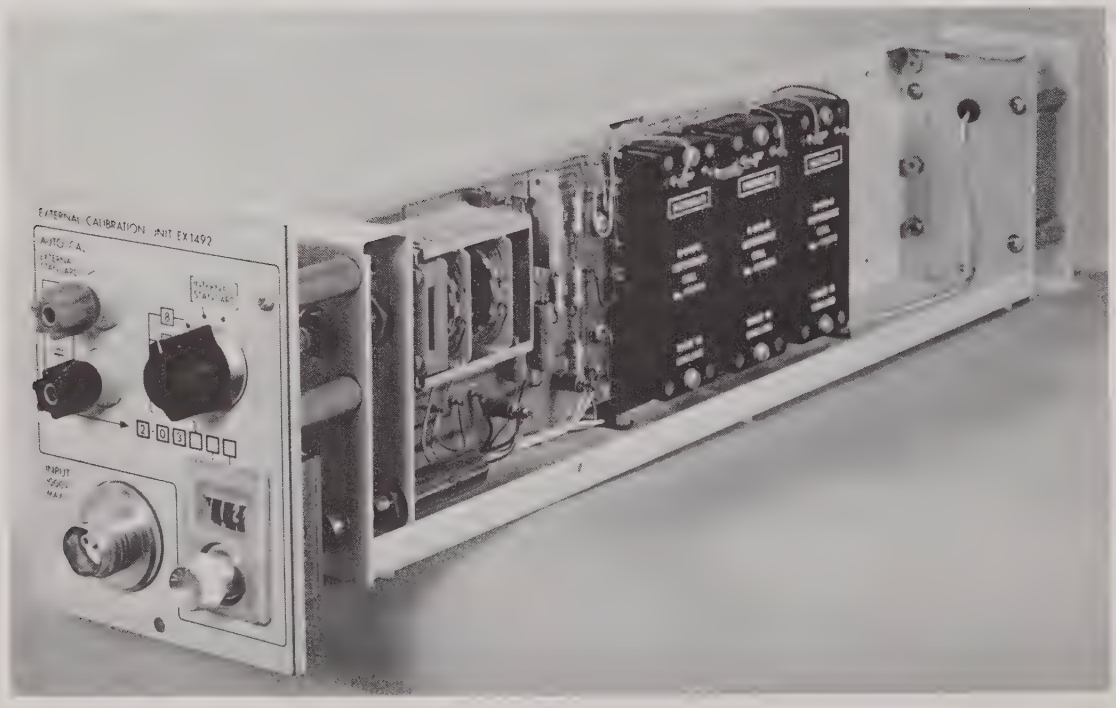


Fig.4.9 External Calibration Unit EX1492

PERFORMANCE CHECK

The following procedure has been extracted from the instruments production test specification to enable the user to verify the performance of LM1490.

APPARATUS REQUIRED

Digital Voltmeter with 10μV resolution	(e.g. Solartron LM1420.2)
Variable Auto Transformer	(e.g. Variac)
Avometer	
Oscilloscope	(e.g. Solartron CD1400)
D.C. Voltage Source. 0-1000V $\pm$ 0.001% $\pm$ ½μV accuracy.	(e.g. Kintel Voltage Standard Type 303B).

PRELIMINARY

Set the controls on the sub-unit so that the instrument can calibrate itself against the internal standard cells.

Switch the instrument on.

1. FRONT PANEL CONTROLS

AUTO/MANUAL

a) Connect the input leads to a low voltage source select a suitable range and press the AUTO push button. Check, by varying the voltage of the source and observing that the reading changes, that the voltmeter automatically updates the display.

b) Press the MANUAL push button. Check that the voltmeter display is updated once only after each successive depression of the MANUAL push button.

INTEGRATION TIME

a) Check that the display scale length and the measurement time increases as the integration time is increased from 2mS to 20mS to 200mS.

b) With 2mS x 2 (LINE SYNC) selected, press the MANUAL push button and check that the measurement time increased compared with the 2mS time only. Similarly, check that with 200mS x 10 selected that the measurement time is approximately 2 seconds.

FILTER 30dB

With a low voltage source connected to the input, a suitable range selected and 20mS INTEGRATION TIME press the AUTO push button. Check when the FILTER 30dB push button is pressed that the reading alters and takes a few seconds to approximate to the previous result.

AUTO RANGE

Select AUTO, 20mS INTEGRATION TIME and AUTO RANGE 200V MAX' Connect a variable low voltage (0 - 30V) source to the input and check the AUTO RANGE facility (check decimal points and units) in both directions (up-ranging and down-ranging). Note that the minimum reading (except on 20mV range) before down-ranging occurs is 020000 and the maximum reading (except on 200V range) before up-ranging occurs is 219999.

MANUAL RANGE

In similar fashion to the above test, check the manual ranges by checking units indication and decimal point position.

DISPLAY

Select AUTO, 200mS and 2V range.

a) Connect the input to a +3V source and from a reading of about +2.00000 adjust the source to check that all numerals from 0 to 9 can be obtained in the 5 least significant decades and 0 to 2 in the most significant decade. Check that the + sign is illuminated.

b) Repeat a) for a negative input and check that the — sign is present.

c) Ensure that the * is displayed for readings of 220000 and greater.

d) With the -3V source connected select the 200mV range and check that the displayed reading is -255.000 *.

e) Change the polarity of the source and check that the displayed reading is +257.000* $\pm$ 20 digits.

f) Select 20mS INTEGRATION TIME and check that the displayed reading is +257.00* $\pm$ 20 digits.

g) Select 2mS INTEGRATION TIME and check that the displayed reading is +257.0* $\pm$ 9 digits.

i) Remove the input voltage and rotate the range switch, checking that the V and mV signs are correctly displayed. In the SUB-UNIT position both mV and V should be extinguished.

AUTO-CAL

Select AUTO and 200mS INTEGRATION TIME. Rear AUTO-CAL switch to INTernal.

Press the CHECK CAL push button and keep it pressed. The displayed reading should be 200 000 $\pm$ 2. Check that the * appears immediately the CHECK CAL button is pressed.

By observing the * indication check that the time between AUTO-CAL operations is 90 sec. $\pm$ 40 sec.

With the rear AUTO-CAL COMMAND switch set to EXTernal, check that the * appears immediately the CHECK CAL switch is pushed and does not occur at any other time.

Return the AUTO-CAL COMMAND switch to INTernal.

2. EXTERNAL FACILITIES

a) Without Fan Out Unit

Range Information

Apply the range commands shown in Table 4.1 and check that the correct range is called by observing the range indication of Table 4.2. Check also the correct decimal point and units indication.

B.C.D.	SKA	20mV	200mV	2V	20V	200V	20V
1	m	0	1	0	1	0	1
2	n	0	0	1	1	0	1
4	p	0	0	0	0	1	1

0 = 0V (Connect to pin HH)
1 = Open Circuit.

Table 4.1 Range Command

B.C.D.	SKA	20mV	200mV	2V	20V	200V
1	f	0	1	0	1	0
2	h	0	0	1	1	0
4	j	0	0	0	0	1

1 = 2.6V to +5V
0 = 0V to +0.4V.

Table 4.2 Range Information

b) With Fan Out Unit EX1488

As a) above and the following.

Display Information

Select AUTO 200mS INTEGRATION TIME and the 2V range.

Using a low (+3V) variable voltage source to display the numbers 1, 2, 4 and 8 in each decade in turn check the corresponding output levels at the pins of rear SKA. Table 4.3 lists the output pins for each decade.

For each decade, only the pin which corresponds to the numeral displayed should be Hi (+5V or +12V depending on linking of Fan Out).

	DECADE					
	10^0	10^1	10^2	10^3	10^4	10^5
1	A	E	K	P	U	Y
2	B	F	L	R	V	Z
4	C	H	M	S	W	–
8	D	J	N	T	X	–

Table 4.3 Display Information - Output

Miscellaneous Information

Select 200mS INTEGRATION TIME, AUTO and 2V range.

Check out the following information as listed in table 4.4.

FUNCTION	PIN	OPERATION	CHECK
PRINT +	d	Measure +1V approx.	+5V at pin d
PRINT –	e	Measure -1V approx.	+5V at pin e
PRINT COMMAND PULSE	u	Press MANUAL	Check for pulse at end of measurement.
PRINT COMMAND LEVEL	v	Select AUTO	0V at pin v
CONTACT SAMPLE	s	Select MANUAL and connect pin s to pin HH	Check that new measurement is made.
PULSE SAMPLE	t	Select MANUAL and apply positive pulse to pin t	Check that new measurement is made.
CLOCK	x	Monitor pin x with oscilloscope	Check that for a 50Hz mains instrument the O/P at pin x is 320kHz (for 60Hz instrument O/P is 384kHz).
AUTO-CAL	y	Connect y to HH	Check that * appears instantly
FILTER	z	Connect z to HH	Check that filter is in circuit.

Table 4.4 Miscellaneous Information

Allow a 'warm-up' time of 1 hour (or 1 day if instrument just received) before proceeding with further checks.

3. Input Current

Select 200mS INTEGRATION TIME, LINE SYNC, AUTO and 200mV range. Connect to the input leads to a network comprising a 1MΩ resistor in parallel with a 1μF capacitor. These components should be fully screened and the screen connected to mains earth. The initial reading should not exceed 250μV. If the display exceeds this value, remove the instrument top cover (as for fan out installation) and adjust RV1 (Current Zero) position 21 for a minimum reading on LM1490.

4. Linearity

Select 200mS INTEGRATION TIME, AUTO and 20V range. Short circuit the input leads. Adjustment of RV1 (Linearity Set Zero) position 22 will enable reading to be set to zero, but it will be necessary to press the CHECK CAL switch before the effect of adjustment can be seen.

Refit the instrument top cover.

5. nV OFFSET

Select 200mS INTEGRATION TIME, LINE SYNC, AUTO and nV ZERO. Check that the range of adjustment of the nV OFFSET control is not less than ± 15μV.

Set the control to give a reading of < ± 1μV.

Short circuit the input leads and select the 20V range. Check that a zero reading is obtained.

Check that zero ± 1 digit is displayed for the 2V, 200V and 1000V ranges.

Press the CHECK CAL switch and keep it pressed. Check that the displayed reading is 200 000 ± 2 digits.

6. Input Resistance

Select 200mS INTEGRATION TIME and AUTO.

Using the voltage standard, check the difference between readings with and without a resistance in series with the Hi input lead as detailed in table 4.5.

Range	Input	Series R	Difference (digits)
20V	+20	1M Ω	20
20V	–20	1M Ω	20
2V	+ 2V	1M Ω	20
2V	– 2V	1M Ω	20
200mV	+200mV	100k Ω	200
200mV	–200mV	100k Ω	200
20V + Filter	+20V	1MΩ (5 min settling	20
20V + Filter	–20V	1MΩ time).	20

Table 4.5 Input Resistance

7. Series Mode Rejection

Select 20mS INTEGRATION TIME and AUTO.

Connect up a supply as shown in figure 4.10 and check that for a 1 digit change in the displayed reading the input voltage is greater than listed in table 4.6.

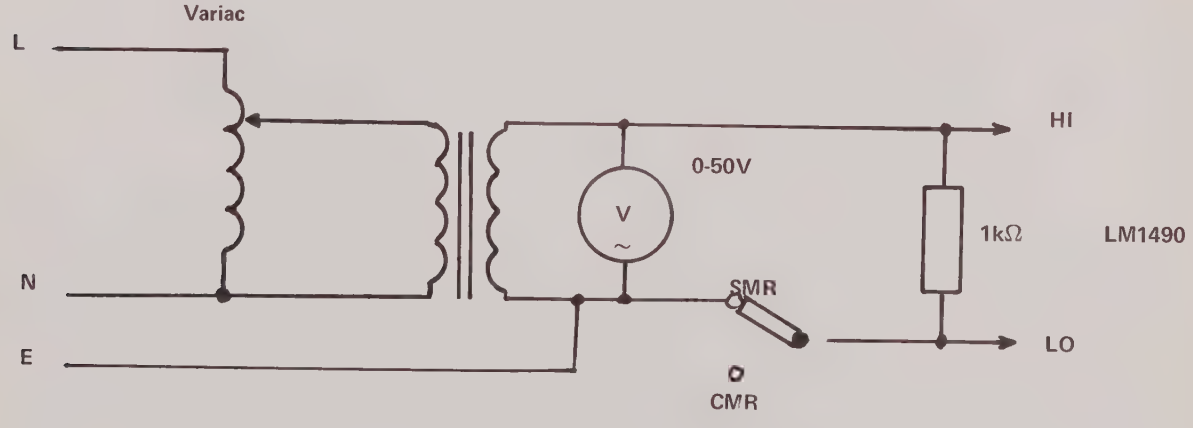


Fig. 4.10 Noise Rejection Test

Range	INTEGRATION TIME	Input Voltage (Without Filter)	Input Voltage (With Filter)
20V	20mS	> 35mV	> 1V
200V	20mS	> 350mV	> 10V
2V	20mS LINE SYNC	> 100mV	> 3.5V

Table 4.6 Series Mode Rejection

8. A.C. Common Mode Rejection

Select 20mS INTEGRATION TIME, AUTO and 200mV range.

Using the circuit of figure 4.10, switch from SMR to CMR and adjust the common mode signal to 1V r.m.s. The reading should not change by more than ± 1 digit.

Select FILTER 30dB and increase the common mode signal to 35V. The reading should not change by more than ± 1 digit.

9. D.C. Common Mode Rejection

Select 200mS INTEGRATION TIME, AUTO, and 200mV range.

Connect LM1490 to the circuit of figure 4.11 and check that the reading is less than 250μV.

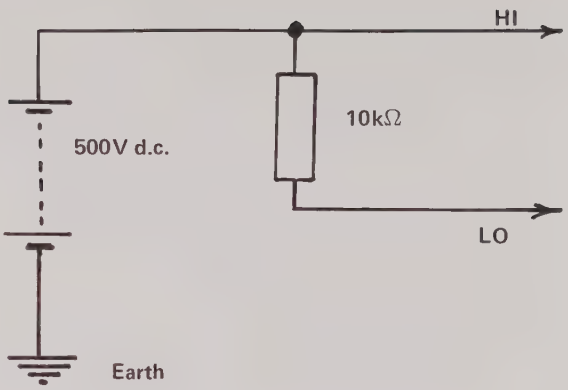


Fig. 4.11

Reduce the common mode voltage to 200V and change the LM1490 range to 200V. Connect mains earth to GUARD and LO and note the displayed reading. Transfer mains earth to input HI and check that the reading settles to within 20 digits of the previous.

Note: The following checks must be carried out in a temperature controlled environment at 20°C. The instrument must be allowed to stabilise at 20°C before starting.

10. Absolute Accuracy

Apply the following inputs to LM1490 and ensure that the reading errors are within the limits shown. The nV OFFSET will require adjusting between the 20mV and 200mV ranges. Use 200mS x 10 when on the 20mV range.

Input \ Ranges	Permitted Error (digits)					
	20V	2V	200mV	20mV	200V	1000V
− 200 000	± 5	± 5	± 6	± 15	± 5	—
− 150 000	± 4	± 4	± 5	± 14	± 4	—
− 100 000	± 3	± 3	± 4	± 13	± 3	± 3
− 50 000	± 2	± 2	± 3	± 12	± 2	± 2
000 000	± 1	± 2	± 2	± 11	± 1	± 1
+ 50 000	± 2	± 2	± 3	± 12	± 2	± 2
+ 100 000	± 3	± 3	± 4	± 13	± 3	± 3
+ 150 000	± 4	± 4	± 5	± 14	± 4	—
+ 200 000	± 5	± 5	± 6	± 15	± 5	—

Table 4.7 Absolute Accuracy

SETTING UP PROCEDURE

The following information is included so that users with the correct facilities can perform routine re-calibration.

APPARATUS REQUIRED

Digital Voltmeter with 10μV resolution (e.g. Solartron LM1420.2)

Oscilloscope (e.g. Solartron CD1400)

D.C. Source 0 - 1000V Accuracy ± 0.001% ± ½μV (e.g. Kintel Voltage Standard type 303G)

D.C. Potentiometer (e.g. Cambridge Instruments Co. Ltd.)

High Voltage Ratio Box 200Ω/V 0.002%

Galvanometer (e.g. Fluke Model 814A)

The latter part of the setting-up procedure must be effected in a temperature controlled environment at 20°C.

PRELIMINARY

Remove the instrument from its case and remove the top and bottom covers of the floating section. Switch on and allow at least 1 hour before making any adjustments.

Rail Adjustment (Positions 1 and 18)

Check that the +18V rail (position 18) is +18.2V ± 0.2V.

Reset RV1 (position 1) if necessary.

Check that the +40V rail (position 1) is +41V ± 3V.

Check that the +5V rail (position 1) is +5V ± 0.2V. Reset RV2 (position 1), if necessary.

Check that the +13V rail is +13V ± 0.7V.

Clock (Position 22)

Monitor the waveform at TP3 (position 22) and adjust T1 core to produce minimum pulse width.

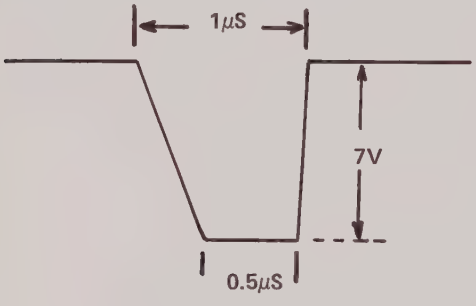


Fig. 4.12 Clock Waveform

Timer Counter (Position 7)

Select AUTO and the 2V range. Short circuit the input leads. Using the oscilloscope, monitor the COUNT bistable waveform at pin 18 of position 10. Measure the following INTEGRATION TIMES and check the displayed reading.

INTEGRATION TIME	Approx. Time	Display
2mS	2mS	0.000--
20mS	20mS	0.0000--
200mS	200mS	0.00000
2mS x 10	2mS	0.000--
2mS x 2	*	0.000--

* A 2mS count initiated every 10mS.

Table 4.8 Integration Times

Input Amplifier (Position 21)

This setting-up procedure need be effected only if the chopper is suspect or a new one is fitted.

Connect pin 1 to pin 2 (position 21) connect a +100mV d.c. source to TP.3 and measure its amplitude (oscilloscope) with respect to pin 2. Transfer the oscilloscope to TP.4 and adjust RV2 to obtain the waveform of figure 4.13.

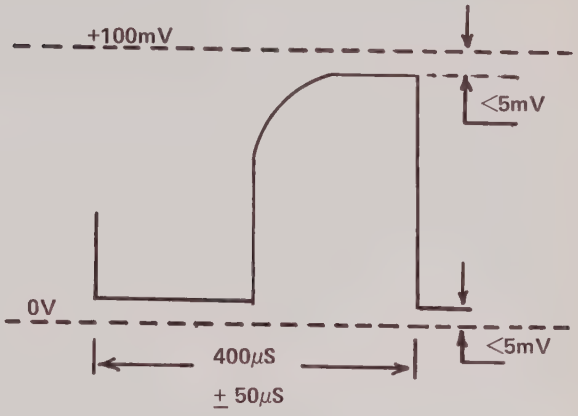


Fig. 4.13 Chopper Waveform

Disconnect pin 1 from pin 2. Measure pin 5 IC1 and remove the link across R54 if voltage exceeds 1.8V.

Monitor TP.2 (oscilloscope. 1mV/cm. 500kHz bandwidth) and adjust RV1 for a minimum spike amplitude (<2mV).

Buffer Amplifier (Position 20)

Select AUTO, 200mS INTEGRATION TIME and 2V range.

Monitor the waveform at TP.2 and adjust C11 for a minimum spike amplitude.

Connect TP.1 and TP.2 (position 22) to 0V. Press the CHECK CAL button and adjust the links on position 20 to give a display of approximately +202 000.

Disconnect TP.1 and TP.2 from 0V.

Using the digital voltmeter monitor the voltages at TP.1 and TP.2. Press the CHECK CAL button until the readings stabilise. Adjust RV1, if necessary, to bring the voltages at TP.1 and TP.2 to within 3V ± 1V.

Q.C.G. Smoothing (Position 23)

With the instrument on the 2V range still, apply an input of -2.4V approx. (from a screened source) and monitor the waveform on pin 14 of position 22. Connect the screen of the low voltage source, the d.v.m. guard and the floating 0V to earth. Trigger the oscilloscope from TP.2 to obtain the waveform shown in fig. 4.14.

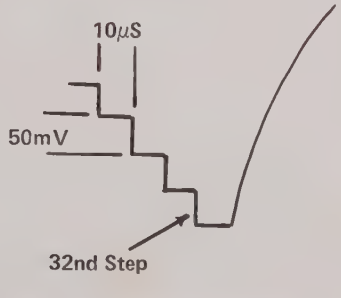


Fig. 4.14 Correction Waveform

Adjust RV1 (position 23) such that the 32nd step of the waveform is of the same amplitude as the previous step.

Monitor TP.1 (position 20) and adjust RV2 (position 23) to obtain a minimum amplitude waveform (<30mV p–p).

Linearity Zero (Position 22)

Select AUTO, 200mS INTEGRATION TIME and 20V range. Short circuit the input leads. Adjustment of RV1 (position 22) will enable the reading to be set to zero but it will be necessary to press the CHECK CAL button before the effect of adjustment will be seen.

Fit the top and bottom covers of the floating box.

Input Current

Select AUTO, 200mS INTEGRATION TIME, LINE SYNC and 200mV range. Connect the input to a network comprising a 1MΩ resistor in parallel with a 1μF capacitor. These components should be fully screened and the screen connected to mains earth. Initial reading on LM1490 should not exceed ± 250μF. Adjust RV1 (position 21) for a minimum reading.

nV OFFSET

Select AUTO, 200mS INTEGRATION TIME, LINE SYNC and nV ZERO. Check that the range of adjustment of the nV OFFSET control is at least ± 15μV.

Reset the control to give a reading of less than ± 1μV.

Final Calibration

The following procedure must be effected in a temperature controlled environment at 20°C after the instrument has been on for at least three hours in this environment. The input LO lead must be connected to earth for all tests and precautions taken to avoid the generation of thermal emf's; e.g. do not use croc. clips, avoid handling connections, etc.

Zero Check

Select; AUTO, 200mS INTEGRATION TIME and LINE SYNC.

Check that with short circuit input, zero is displayed on the 200mV to 1000V.

Range Set-Up

The following set up is only a typical arrangement and is not mandatory. The main requirement is that the equipment used should have a known accuracy.

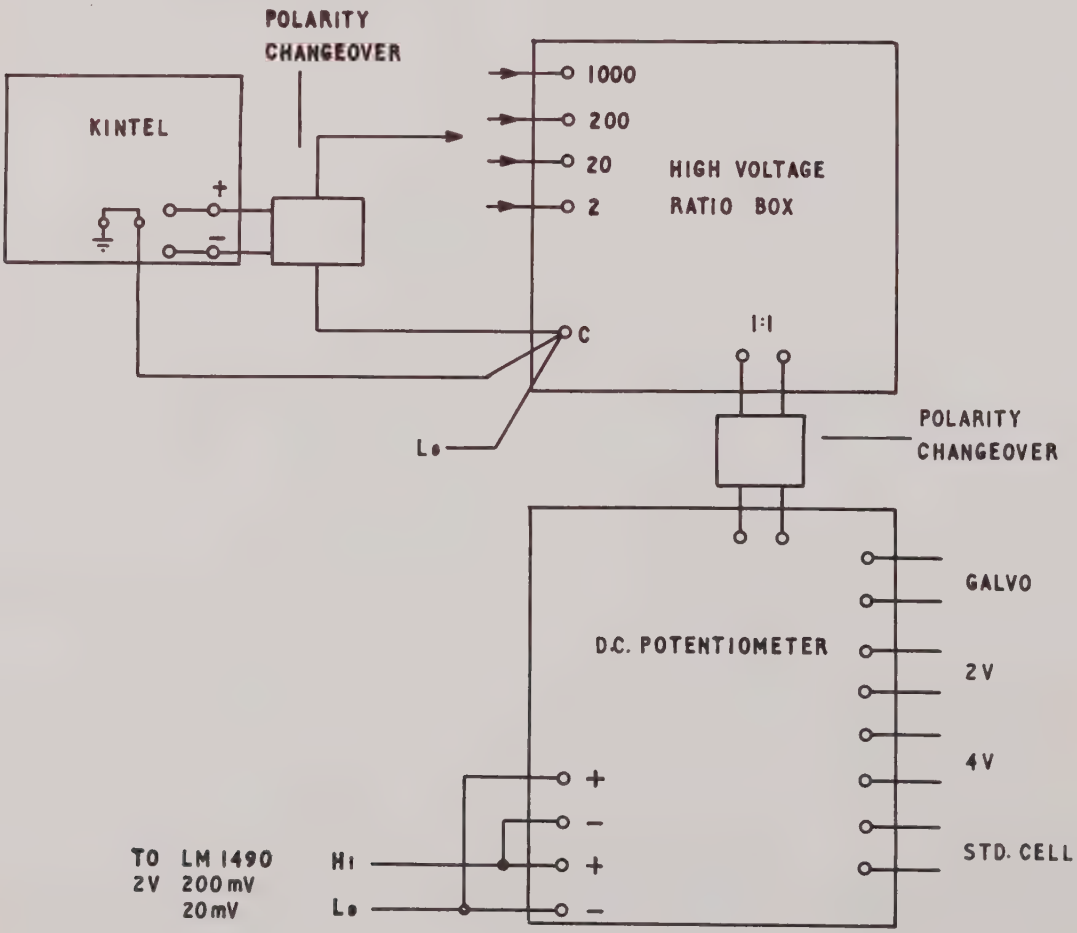


Fig. 4.15

Select; AUTO, 200mS INTEGRATION TIME.

Set the output of the Kintel to −20.0000V and connect to the 20V input of the High Voltage Ratio Box. Connect the Hi input of LM1490 to the 20V input on the ratio box (LO is connected to Earth). Set the dials on the DC Potentiometer to 2.0000000V and adjust the Kintel for a null on the galvanometer. Note the reading on LM1490. Change the output of the Kintel to −2.00000V and connect to the 2V input of High Voltage Ratio Box. Change to the 2V range on LM1490 and connect HI to the 2V input on the H.V. Ratio Box. Readjust the Kintel output for a null on the galvanometer and adjust RV4 position 17 for the same reading as that obtained on the 20V range.

Connect the Kintel output to the 200V input on the H.V. Ratio Box and change the output to 200V. Change to the 200V range on LM1490 and connect Hi to the 200V input on the H.V. Ratio Box. Adjust the Kintel output for a null on the galvanometer and adjust RV1 position 17 to obtain the 2V reading.

Reduce the Kintel output to 2V and connect to the 2V input on the H.V. Ratio Box. Using the d.c. potentiometer as a voltage source apply −2.0000V to the LM1490 (on 2V range) and note the display reading. Change to the 200mV range and change the potentiometer output to −200mV. Adjust RV3 position 17 to obtain the 2V range reading.

Apply −20mV on the 20mV range and adjust RV2 position 17 to obtain the 200mV range reading.

Repeat the procedure using both negative and positive inputs and sharing the errors if necessary. It may be necessary to reset the nV OFFSET before calibrating the 20mV range.

External Standardisation

Note: If the user does not possess an EX1492 this procedure cannot be effected.

Connect a pair of standard cells (whose sum voltages lie between 2.03800V and 2.03900V known to an accuracy of 0.0005%) to the terminals of EX1492. Arrange the controls to equal the absolute value of the standard cells. Monitor −2.03900V, from the d.c. potentiometer, on the 2V range of LM1490. Press the CHECK CAL button and adjust RV5 position 17 alternately, until the LM1490 displays −2.03900V.

Internal Standard

Monitor −2.03900V from the d.c. potentiometer on the 2V range of LM1490 (using internal standard). Alternatively press CHECK CAL and adjust RV1 on the sub-unit until LM1490 displays −2.03900V. Repeat for +2.03900V and share the difference in readings.

Absolute Accuracy

Apply the following inputs to LM1490 and ensure that the reading errors are within the limits shown. The nV OFFSET will require repositioning between the 200mV and 20mV range. Use 200mS x 10 when operating on the 20mV range.

Input \ Ranges	Permitted Error (digits)					
	20V	2V	200mV	20mV	200V	1000V
−200 000	± 5	± 5	± 6	± 15	± 5	—
−150 000	± 4	± 4	± 5	± 14	± 4	—
−100 000	± 3	± 3	± 4	± 13	± 3	± 3
− 50 000	± 2	± 2	± 3	± 12	± 2	± 2
000 000	± 1	± 2	± 2	± 11	± 1	± 1
+ 50 000	± 2	± 2	± 3	± 12	± 2	± 2
+100 000	± 3	± 3	± 4	± 13	± 3	± 3
+150 000	± 4	± 4	± 5	± 14	± 4	—
+200 000	± 5	± 5	± 6	± 15	± 5	—

Table 4.9 Absolute Accuracy

Sub-Units

EX1491: As for Internal Standard.

EX1492: Plug the EX1492 into LM1490. Switch to external standard (8,7,6 or 5). Connect a D.V.M. between pin 3 and pin 8 (on P.C.B.) and adjust RV2 for 4.00mV.

Switch to internal standard and press CHECK CAL.

Connect two standard cells (whose sum voltages lie between 2.038V and 2.039V known to an accuracy of 0.0005%) to the external reference terminals.

Select AUTO, 200mS INTEGRATION TIME and 2V range.

Monitor the external cells on LM1490 (negative polarity). Alternately press CHECK CAL and adjust RV1 (EX1492) until LM1490 displays the value of the standard cell.

Switch to external reference and set the controls of EX1492 to 2.03890. Press CHECK CAL and measure the standard cell voltage on LM1490 (negative polarity). The reading should be 2.03890 ± 2 digits.

Switch the EX1492 dials to the following settings, press CHECK CAL after each setting and observe the LM1490 readings.

Control Setting	LM1490 Display
2.03850	−2.03850 ± 2 digits
2.03750	−2.03750 ± 2 digits
2.03650	−2.03650 ± 2 digits
2.03550	−2.03550 ± 2 digits
2.03510	−2.03510 ± 2 digits

Re-adjustment of RV2 may be required to optimise the readings.

CIRCUIT DIAGRAMS

AND COMPONENT PARTS LISTS

Component Parts List
Abbreviations

Circuit References	
R	Fixed Resistor [Ω]
RNL	Non Linear Resistor [Ω]
RV	Variable Resistor [Ω]
C	Capacitor [μF]
MR	Diode
L	Inductor
V	Valve
VT	Transistor
IC	Integrated Circuit
RL	Relay
S	Switch
PL	Plug
SK	Socket
MSP	Mains Selector Panel
T	Transformer
FS	Fuse
ILP	Lamp
B	Battery
M	Meter
TP	Terminal Post
LK	Link
X	Other Components

Component Composition	
A	Capacitor Polystyrene Tubular
B	Capacitor Polyester Tubular Metalised
C	Capacitor Polyester Tubular Foil
D	Capacitor Paper Foil
E	Capacitor Paper Metalised
F	Capacitor Ceramic Tubular
G	Capacitor Ceramic Disc
H	Capacitor Silver Mica
J	Capacitor Electrolytic Al.
K	Capacitor Electrolytic Al. Plain Foil
L	Capacitor Electrolytic Tantalum
M	Capacitor Variable Air Preset
N	Capacitor Variable Ceramic Disc Preset
P	Capacitor Variable Tubular Preset
R	Capacitor Variable Mica Compression Preset
S	Capacitor Polyester Special
T	Capacitor Polycarbon
V	Resistor Metalised Film
W	Resistor Composition <5%
X	Resistor Composition >5%
Y	Resistor Wire Wound
Z	Resistor Oxide Film >5%

Units and Values			
A	Amp	G	Giga [10^9]
F	Farad	M	Mega [10^6]
H	Henry	k	kilo [10^3]
Ω	Ohm	m	milli [10^{-3}]
V	Volts	μ	micro [10^{-6}]
W	Watts	p	pico [10^{-12}]

ACCESSORIES

Cable, Input	359900010
Clips, Alligator	355900150
Prod. Test Black	351901010
Prod Test Red	351901020
Fuse 1 Slo Blo	360105080
Fuse 50mA Slo Blo	360105060
Plug Conn. Free 50 way	354002340
Conn. Pin Bandomatic	354003280

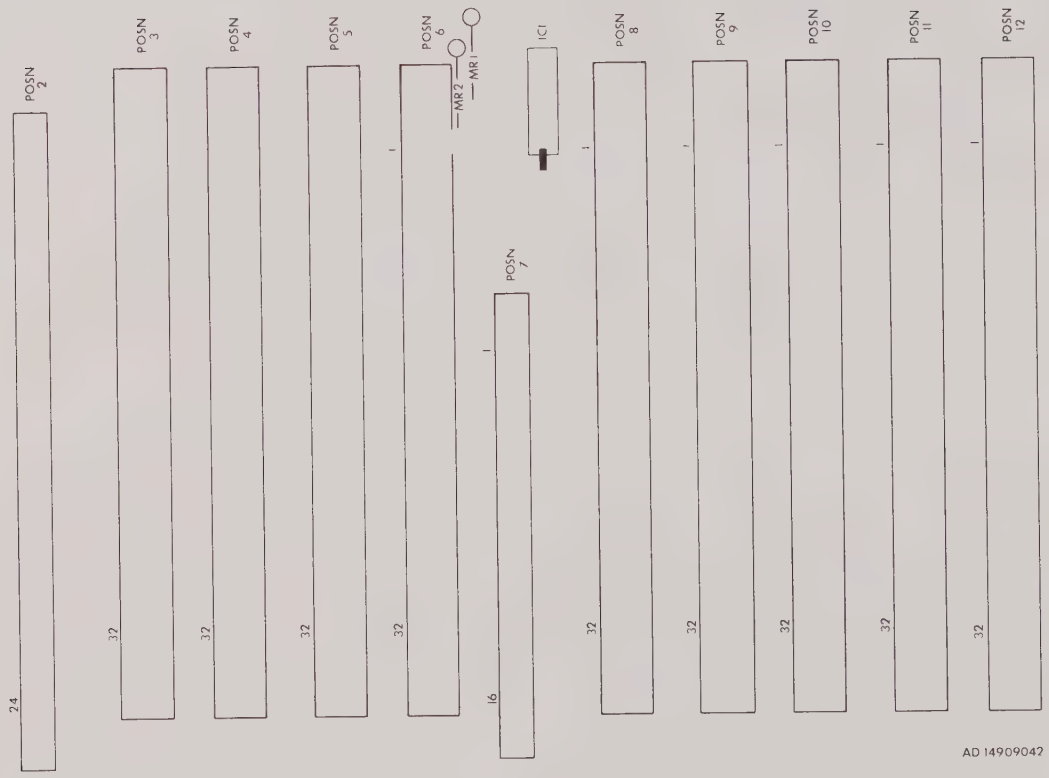
EARTHY SECTION ASSEMBLY

Cct. Ref.		General Description			Solartron Part No.
VT1 to VT3		2N3055			300552340
R1	Y	150	12W	5%	174321500
R2	Y	150	12W	5%	174321500
R3	X	470	¼W	10%	172324700
R4	Y	4.7	6W	5%	355400110
R5	X	220k	½W	10%	172352200
R6	Z	51k	1W	5%	193445100
R7	Z	51k	1W	5%	193445100
R8	Z	100k	½W	5%	193551000
R9	Z	100k	½W	5%	193551000
R11	X	5.6k	1/8W	10%	172035600
R12	X	1M	¼W	10%	172361000
R13	X	1M	¼W	10%	172361000
C1		2000	70V	-20% +50%	208600052
C2		500	50V	-20% 50%	271185000
C3		2000	25V	-20% 50%	208600178
C5		5000	15V	-20% +50%	208600144
C6		5000	15V	-20% +50%	208600144
C8		16	350V	-20% +50%	262371600
C9		2000	25V	-20% +50%	208600178
C10		500	12V	-20% +50%	270485000
C11		4700p	350V	25%	208400059
C12		0.047	630V	20%	208300059
C13		0.047	630V	20%	208300059
S.A.		Switch Push-Button			B14900214
S.B.		Switch Push-Button			B14900064
S.D.		Switch D.P. On/Off			376000530
ILP1 to ILP4		Neon Ind. 16 L			300720140
ILP5 to ILP7		Neon indicator L1166			300720300

Cct. Ref.	General Description		Solartron Part No.
	Fuse 500mA Slo-Blo		360105060
	Fuse Holder		360203070
	Mains 3 Core Cable		480140200
	Switch Slider S.P.D.T.		375000100
	Knobs Push Button Switch		379900960
T1	Transformer Assembly.		AD14900274
MR1 to MR6	ISO23		300524200
MR7	RAS310 AF		300522870
MR8	RAS310 AF		300522870
MR9	ISO23		300524200
MR10	ISO23		300524200
MR11	SD3	Solartron	300551650
MR12	SD3	Solartron	300551650
MSP1	Main Selector Panel		399000060
SKA	Conn. Fixed 50 Way (Shell)		354002330
PLB	Conn. Plug 32 Way		352332050
SKC	Conn. Skt. 24 Way		352524260

COUNTER MOTHER BOARD

Cct. Ref.	General Description	Solartron Part No.
MR1	SD3	300522160
MR2	SD3	300522160
IC1	861 Dual 4 Input Gate	510000360



FLOATING BOX ASSEMBLY

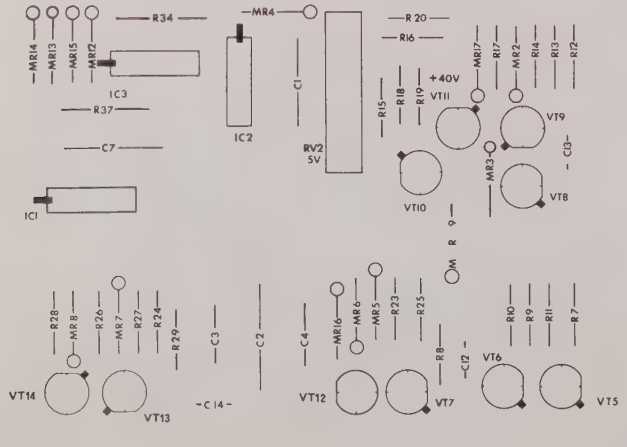
Cct. Ref.	General Description	Solartron Part No.	Cct. Ref.	General Description	Solartron Part No.
SKB	Conn. Socket 32 Way	352532210	SKD	Conn. Socket 16 Way	352516180
RV1	10k 1W 5%	B14900029	SC	Switch Range	B14900107

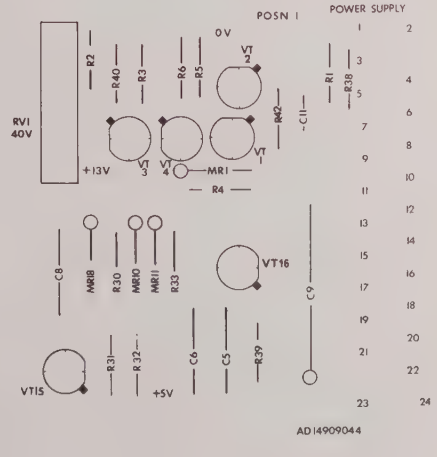
POWER SUPPLY P.C.B. (POSITION NO. 1)

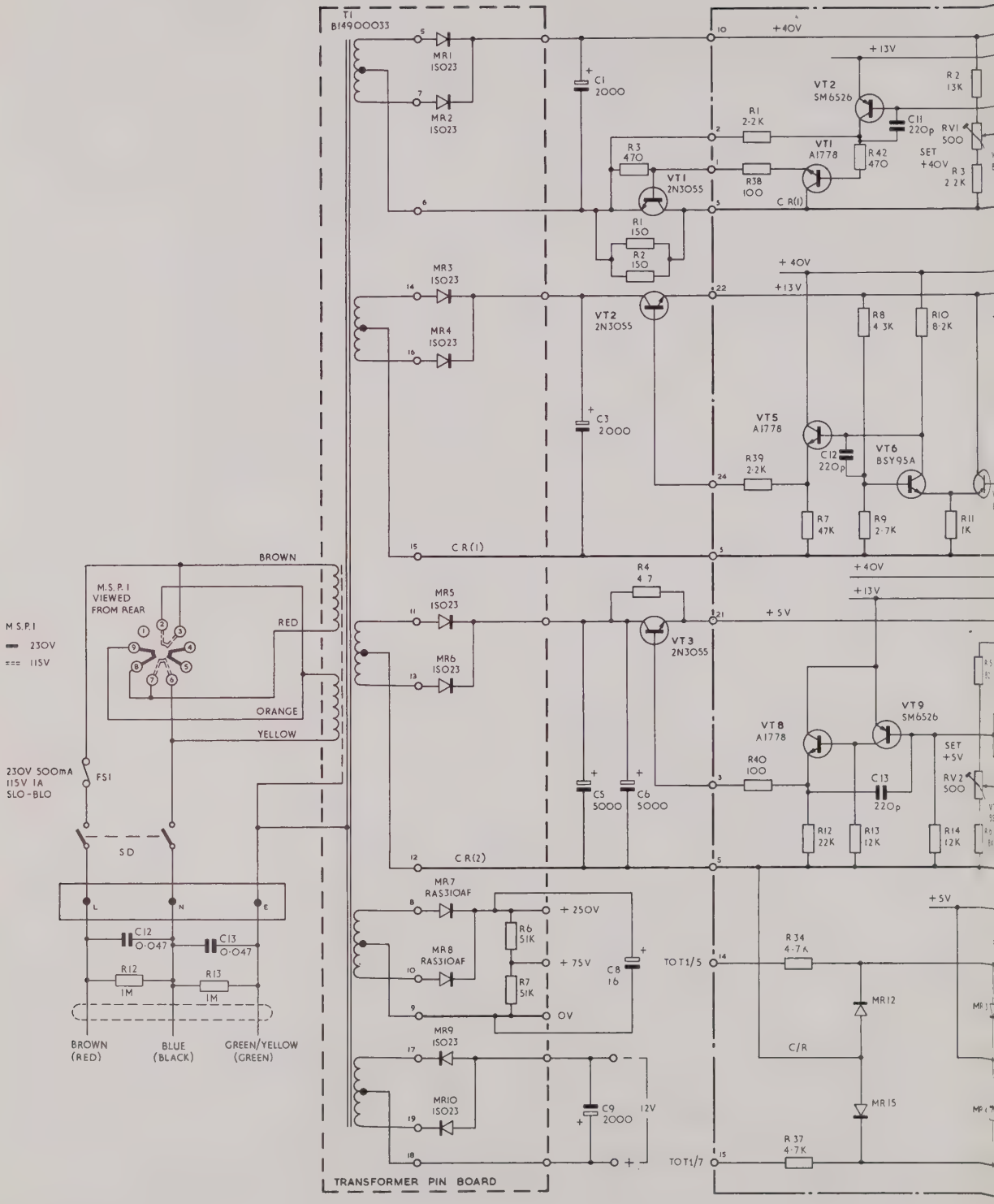
Cct. Ref.		General Description			Solartron Part No.
R1	X	2200	½W	10%	172332200
R2	X	13k	½W	1%	195441300
R3	Z	2200	½W	1%	195432200
R4	X	1200	½W	10%	172331200
R5	X	12k	½W	10%	172341200
R6	Z	4700	½W	1%	195434700
R7	X	47k	½W	10%	172344700
R8	Z	4300	½W	1%	195434300
R9	Z	2700	½W	1%	195432700
R10	X	8200	½W	10%	172338200
R11	X	1000	½W	10%	172331000
R12	X	22k	½W	10%	172342200
R13	X	12k	½W	10%	172341200
R14	X	12k	½W	10%	172341200
R15	Z	82	½W	1%	195418200
R16	Z	1800	½W	1%	195431800
R17	X	1000	½W	10%	172331000
R18	X	15k	½W	10%	172341500
R19	Z	6800	½W	1%	195436800
R20	X	10k	½W	10%	172341000
R23	X	10k	½W	10%	172341000
R24	X	8200	½W	10%	172338200
R25	X	150M	1/10W	20%	160000235
R26	X	47k	½W	10%	172344700
R28	X	5600	½W	10%	172335600
R29	X	5600	½W	10%	172335600
R27	X	22k	½W	10%	172342200
R30	X	27k	½W	10%	172342700
R31	X	4700	½W	10%	172334700
R32	X	4700	½W	10%	172334700
R33	X	27k	½W	10%	172342700
R34	Z	4700	1W	1%	193434799
R37	Z	4700	1W	1%	193434700
R38	X	100	½W	10%	172321000
R39	X	2200	½W	10%	172332200
R40	X	100	½W	10%	172321000
R42	X	470	¼W	10%	172324700
RV1		500	¼W	10%	122025000
RV2		500	¼W	10%	122025000

Cct. Ref.	General Description			Solartron Part No.
C1	.01	400V	10%	220841000
C2	0.33	160V	10%	220353300
C3	1.0	100V	10%	225461000
C4	0.47	100V	10%	225454700
C5	2200p	160V	10%	221332200
C6	2200p	160V	10%	221332200
C7	.1	160V	10%	220351000
C8	0.1	160V	10%	220351000
C9	100	25V	-20% +100%	270781000
C11 to C13	220p	500V	10%	208400046
C14	1500p	500V	10%	208400087

MR1	SZD6.2	Solartron	300521240
MR2	SD2	Solartron	300522160
MR3	SD2	Solartron	300522160
MR4	SZD4.3	Solartron	300523900
MR5 to MR16	SD2	Solartron	300522160
MR17	SZD4.3	Solartron	300523900
MR18	HG5009		300520560
VT1	A1778		300551430
VT2	SM6526		300552990
VT3	BSY95A		300552280
VT4	BSY95A		300552280
VT5	A1778		300551430
VT6	BSY95A		300552280
VT7	BSY95A		300552280
VT8	A1778		300551430
VT9	SM6526		300552990
VT10	BSY95A		300552280
VT11	BSY95A		300552280
VT12	F.E.T. 2N3819		300553220
VT13 to VT16	BSY95A		300552280
IC1	IC936 Hex-Inverter		510000290
IC2	IC946 Quad 2 I/P gate		510000160
IC3	IC962 Triple 3 I/P gate		510000200

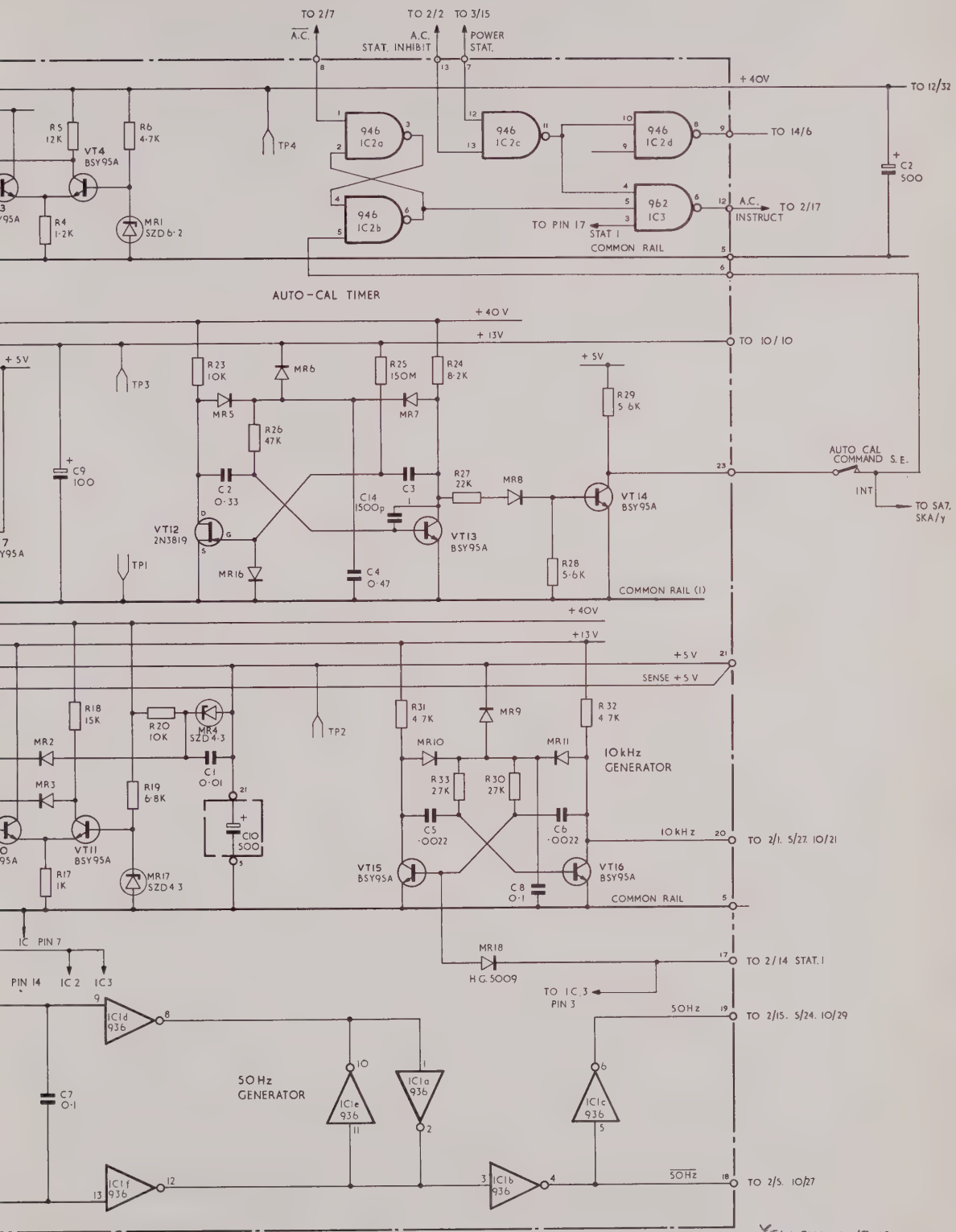






NOTE

1. ALL DIODES TO BE TYPE SD3 UNLESS OTHERWISE STATED
2. PIN DESTINATIONS SHOWN POSN/PIN e.g. 2/5 INDICATES POSN 2 PIN 5



YELLOW = M.M.
GREEN = B.B.
MAUVE = C.C.
WHITE = D.D.
RED = +13V

5. PIN 22 (BD1)

AA, BB C.C.
2mS 20mS 200mS

TO SOCKET.

AA BB CC 3.

FROM

integ common (was 4)

02 29-3-71

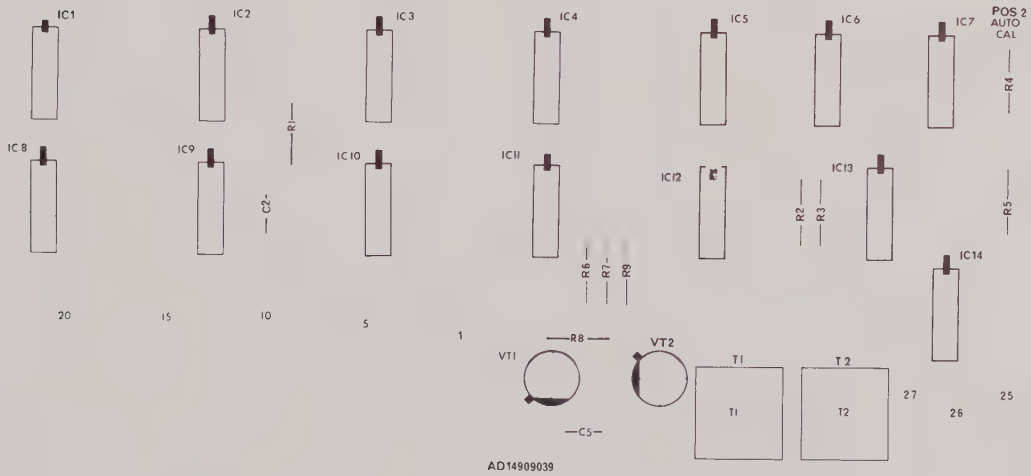
D14909344

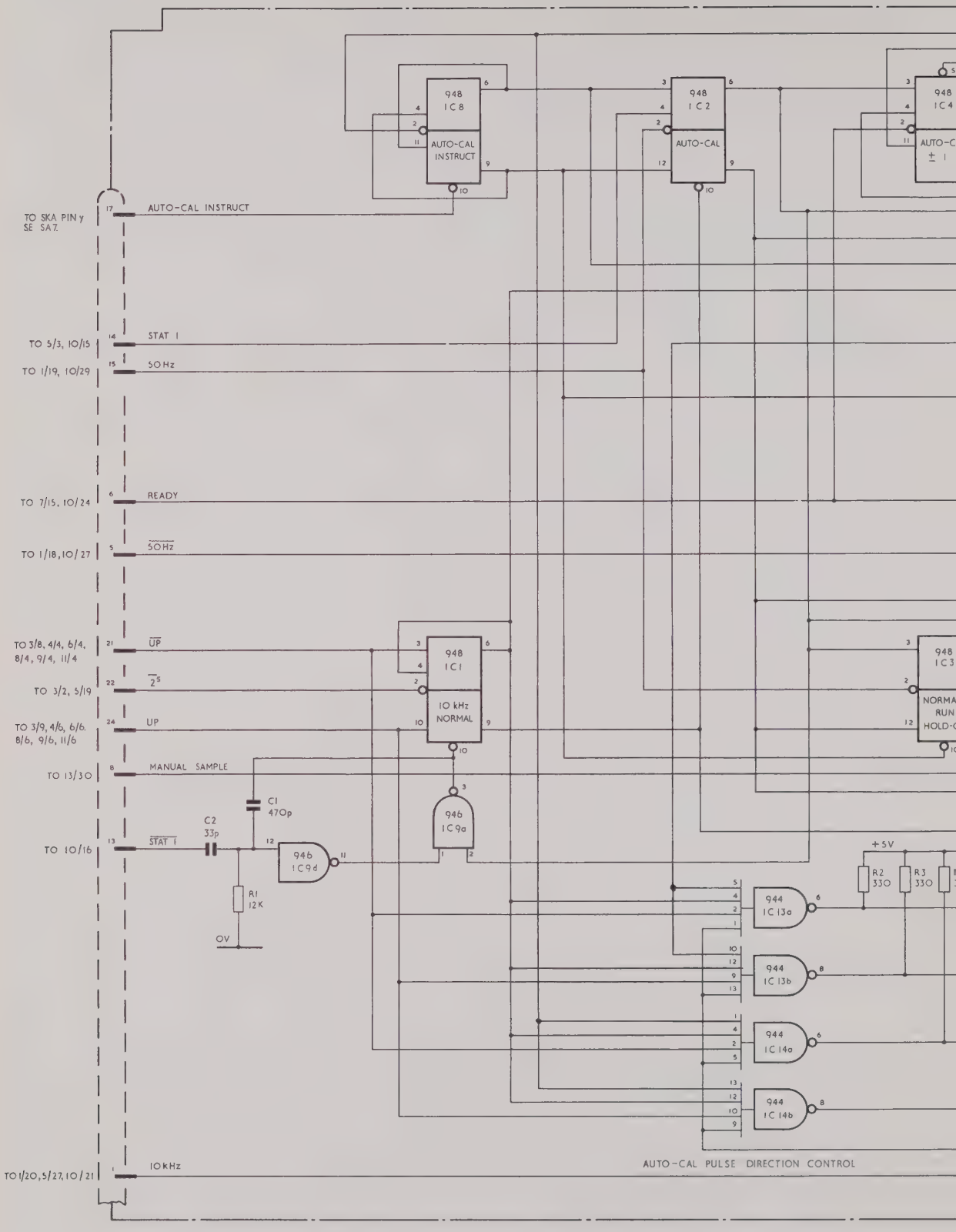
1490 POWER SUPPLY. POSITION 1

AUTO-CAL LOGIC P.C.B. (POSITION NO. 2)

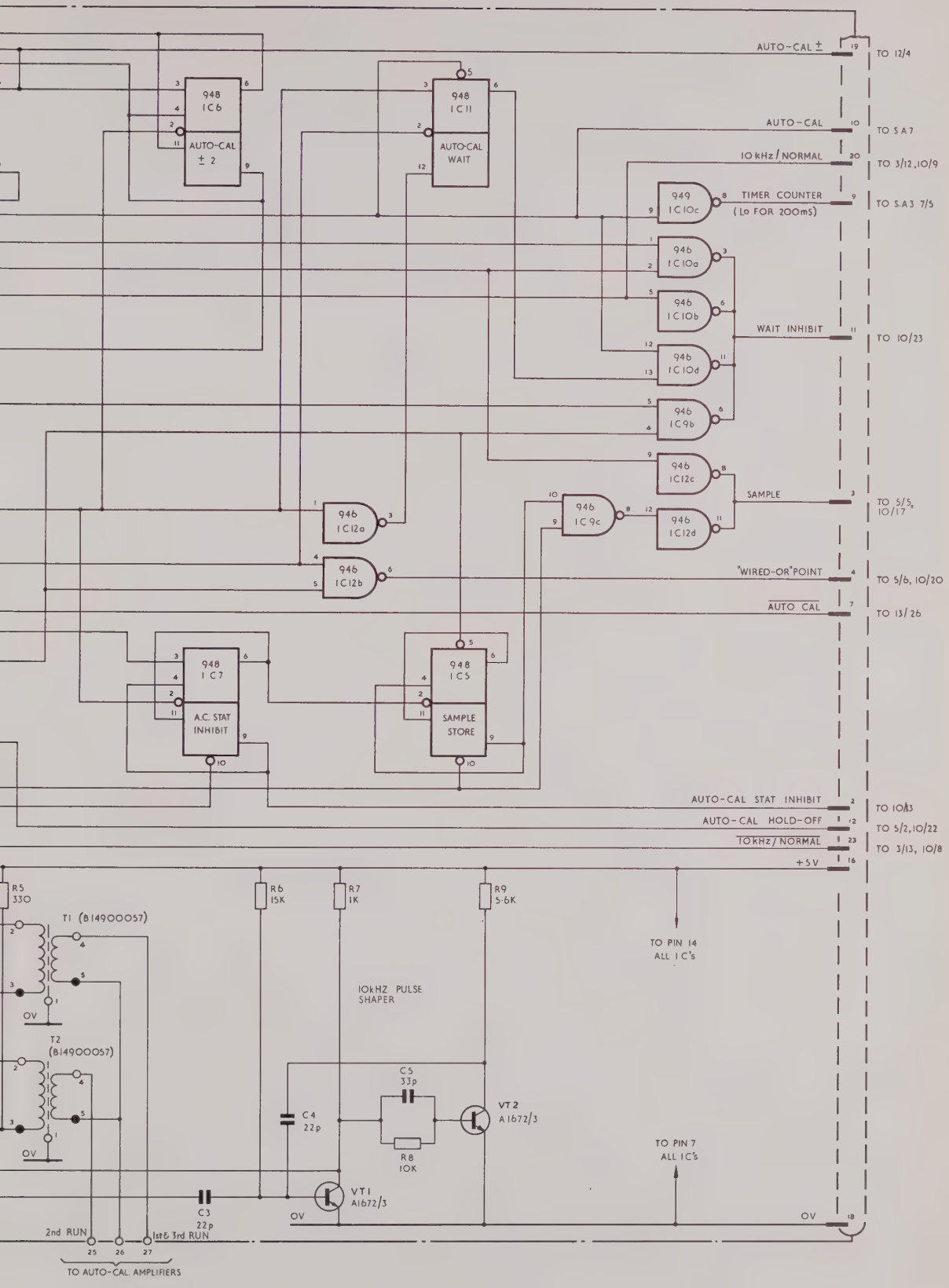
Cct. Ref.		General Description			Solartron Part No.
R1	X	12k	½W	10%	172341200
R2 to R5	X	330	½W	10%	172323300
R6	X	15k	½W	10%	172341500
R7	X	1000	½W	10%	172331000
R8	X	10k	½W	10%	172341000
R9	X	5600	½W	10%	172335600
C1		470p	500V	10%	208400084
C2		33p	750V	10%	208400088
C3		22p	750V	10%	240412200
C4		22p	750V	10%	240412200
C5		33p	760V	10%	208400088

Cct. Ref.	General Description	Solartron Part No.
IC1 to IC8	948 Clocked Flip-Flop	510000170
IC9	946 Quad 2 Input Gate	510000160
IC10	946 Quad 2 Input Gate	510000160
IC11	948 Clocked Flip-Flop	510000170
IC12	946 Quad 2 Input Gate	510000160
IC13	944 Dual 4 Input Power Gate	510000140
IC14	944 Dual 4 Input Power Gate	510000140
VT1	A1672/3	300551910
VT2	A1672/3	300551910
T1	Transformer Pulse	B14900057
T2	Transformer Pulse	B14900057





NOTE
PIN DESTINATIONS SHOWN AS POS^{N}/PIN
e.g. 3/15 INDICATES POS^{N} 3 PIN 15
FOR DESTINATIONS NOT SHOWN SEE
MOTHER BOARD CONNECTIONS



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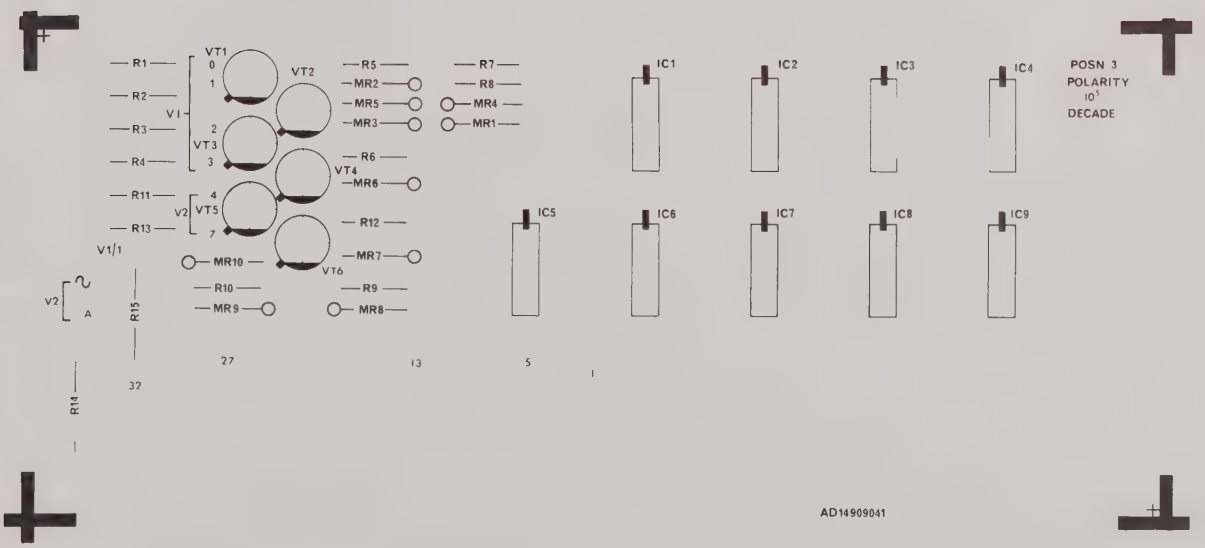
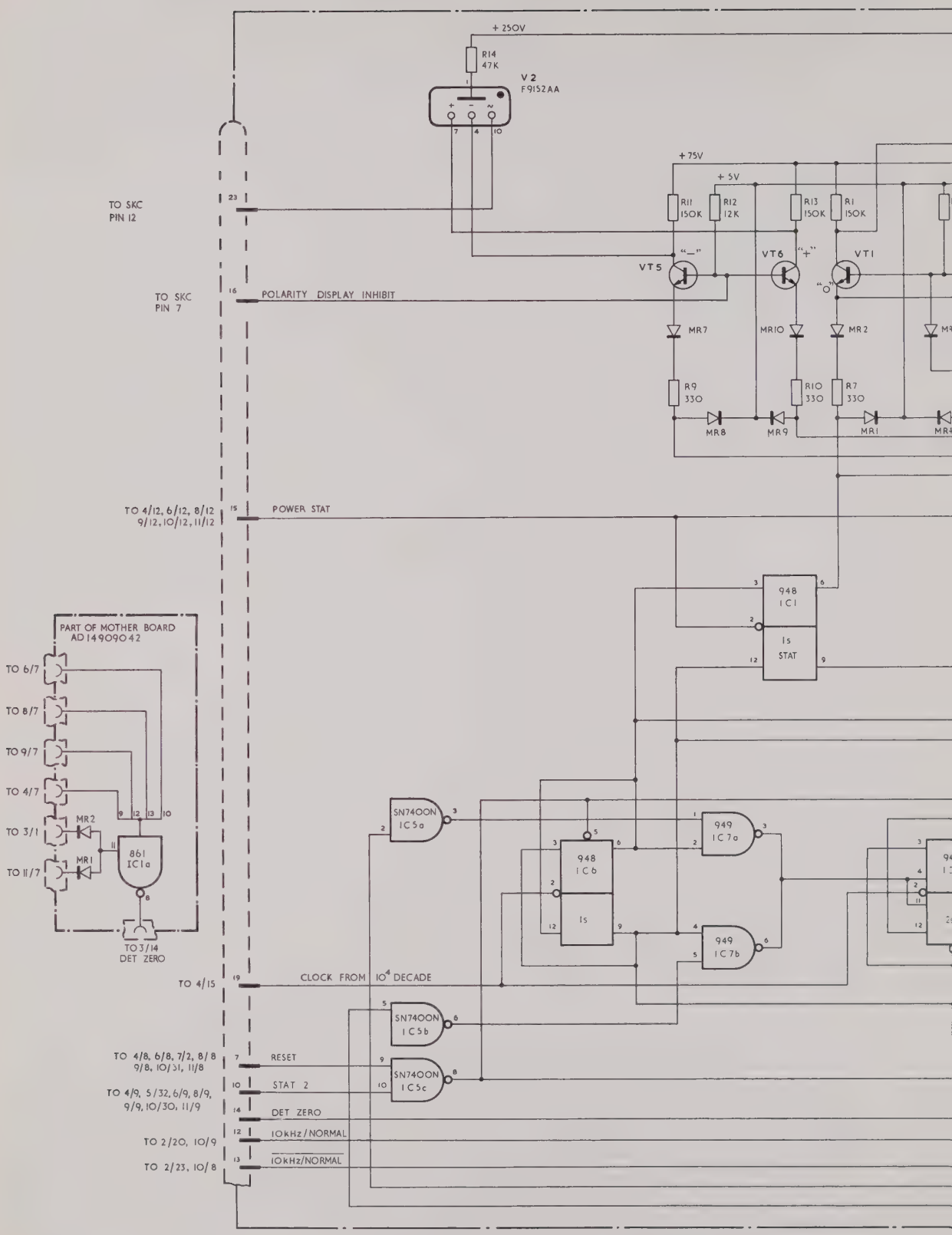
AUTO-CAL LOGIC. POSITION 2

10^5 REVERSIBLE DECADE P.C.B. (POSITION NO. 3)

Cct. Ref.		General Description			Solartron Part No.
R1 to R4	X	150k	½W	10%	172351500
R5	X	12k	½W	10%	172341200
R6	X	12k	½W	10%	172341200
R7 to R10	X	330	½W	10%	172323300
R11	X	150k	½W	10%	172351500
R12	X	12k	½W	10%	172341200
R13	X	150k	½W	10%	172351500
R14	Z	47k	1W	5%	193444700
R15	Z	47k	1W	5%	193444700
MR1 to MR10		SD3			300522160

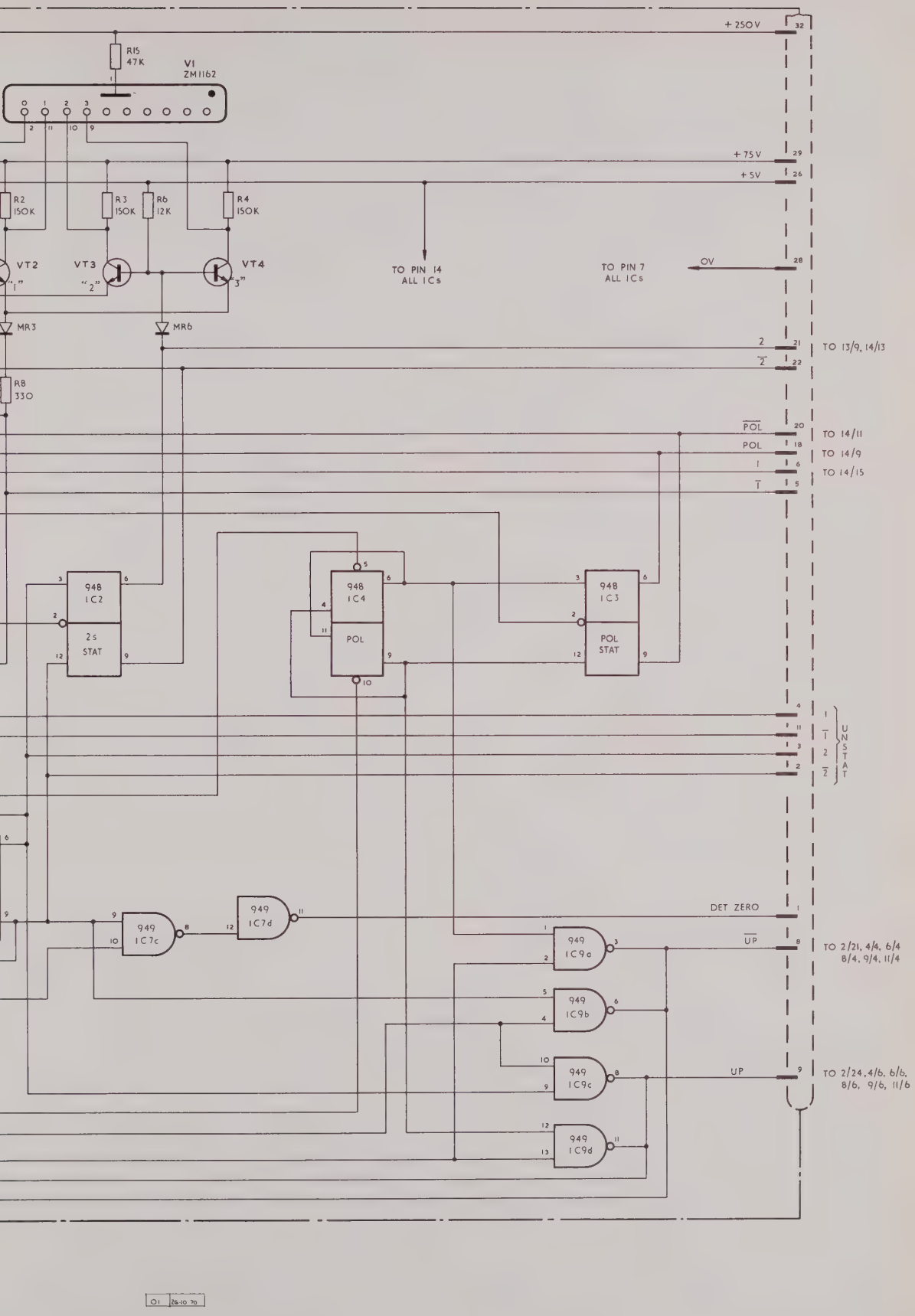
Cct. Ref.	General Description	Solartron Part No.
VT1 to VT6	A1778/2	300551430
IC1 to IC4	948 Clocked Flip-Flop	510000170
IC5	SN7400N Quad 2 Input Gate	510000340
IC6	948 Clocked Flip-Flop	510000170
IC7	849 Quad 2 Input Gate	510000370
IC8	948 Clocked Flip-Flop	510000170
IC9	849 Quad 2 Input Gate	510000370
V1	ZM1162	300011370
V2	F9152AA	300011380





NOTE
1. ALL DIODES TO BE SD3
2. ALL TRANSISTORS TO BE A1778/2

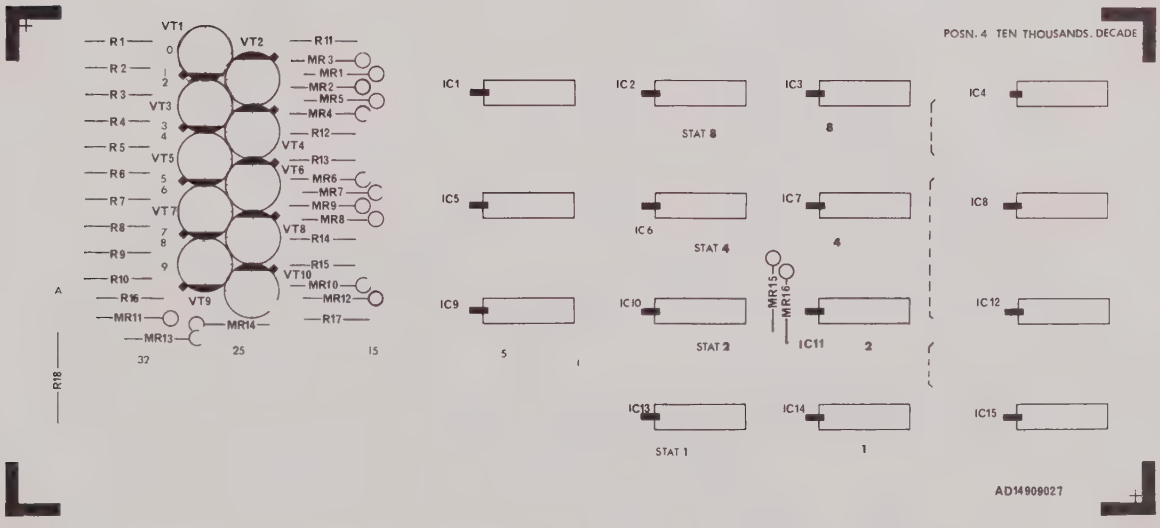
PIN DESTINATIONS SHOWN AS POS^{N}/PIN
e.g. 3/15 INDICATES POS^{N} 3 PIN 15
FOR DESTINATIONS NOT SHOWN SEE MOTHER BOARD CONNECTIONS


+250V
32
R15
47K
V1
ZM1162
+75V
29
+5V
26
R2
150K
R3
150K
R6
12K
R4
150K
VT2
"1"
VT3
"2"
VT4
"3"
TO PIN 14
ALL ICs
TO PIN 7
ALL ICs
0V
28
MR3
MR6
R8
330
2
21
TO 13/9, 14/13
$\overline{2}$
22
$\overline{POL}$
20
TO 14/11
POL
18
TO 14/9
1
6
TO 14/15
$\overline{1}$
5
948
1C2
2s
STAT
948
1C4
POL
948
1C3
POL
STAT
1
$\overline{1}$
2
$\overline{2}$
UNSTAT
949
1C7c
949
1C7d
DET ZERO
1
$\overline{UP}$
8
TO 2/21, 4/4, 6/4
8/4, 9/4, 11/4
949
1C9a
949
1C9b
949
1C9c
UP
9
TO 2/24, 4/6, 6/6,
8/6, 9/6, 11/6
949
1C9d
01
26-10-70

REVERSIBLE DECADE COUNTER. POSITIONS 4, 6, 8, 9 AND 11

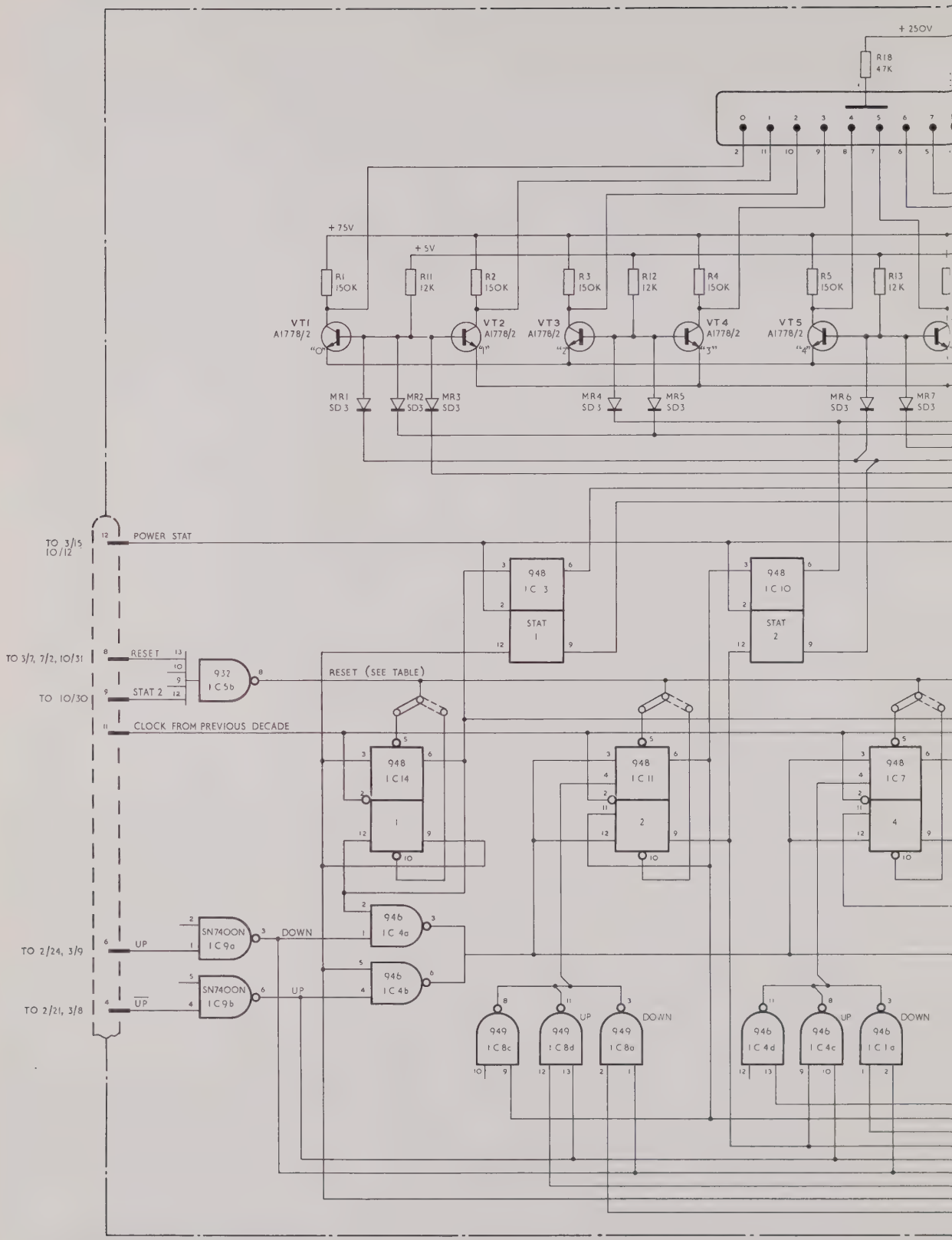
Cct. Ref.		General Description			Solartron Part No.
R1 to R10	X	150k	½W	10%	172351500
R11 to R15	X	12k	½W	10%	172341200
R16	X	330	½W	10%	172323300
R17	X	330	½W	10%	172323300
R18	Z	47k	1W	5%	193444700
MR1 to MR16		SD3		Solartron	300522160
VT1 to VT10		A1778/2			300551430

Cct. Ref.	General Description	Solartron Part No.
V1	Valve ZM1162	300011370
IC1	IC946 Quad 2 Input Gate	510000160
IC2	IC948 Clocked Flip-Flop	510000170
IC3	IC948 Clocked Flip Flop	510000170
IC4	IC946 Quad 2 Input Gate	510000160
IC5	IC932 Dual Buffer	510000120
IC6	IC948 Clocked Flip-Flop	510000170
IC7	IC948 Clocked Flip-Flop	510000170
IC8	IC849 Quad 2 Input Gate	510000370
IC9	IC SN7400N Quad 2 Input Gate	510000340
IC10	IC948 Clocked Flip-Flop	510000170
IC11	IC948 Clocked Flip-Flop	510000170
IC12	IC SN7420N Dual Buffer	510000380
IC13	IC948 Clocked Flip-Flop	510000170
IC14	IC948 Clocked Flip-Flop	510000170
IC15	IC861 Dual Four Input Gate	510000360
	Conn. Plug 32 Way	352332040



INDICATOR TUBE BRACKET ASSEMBLY

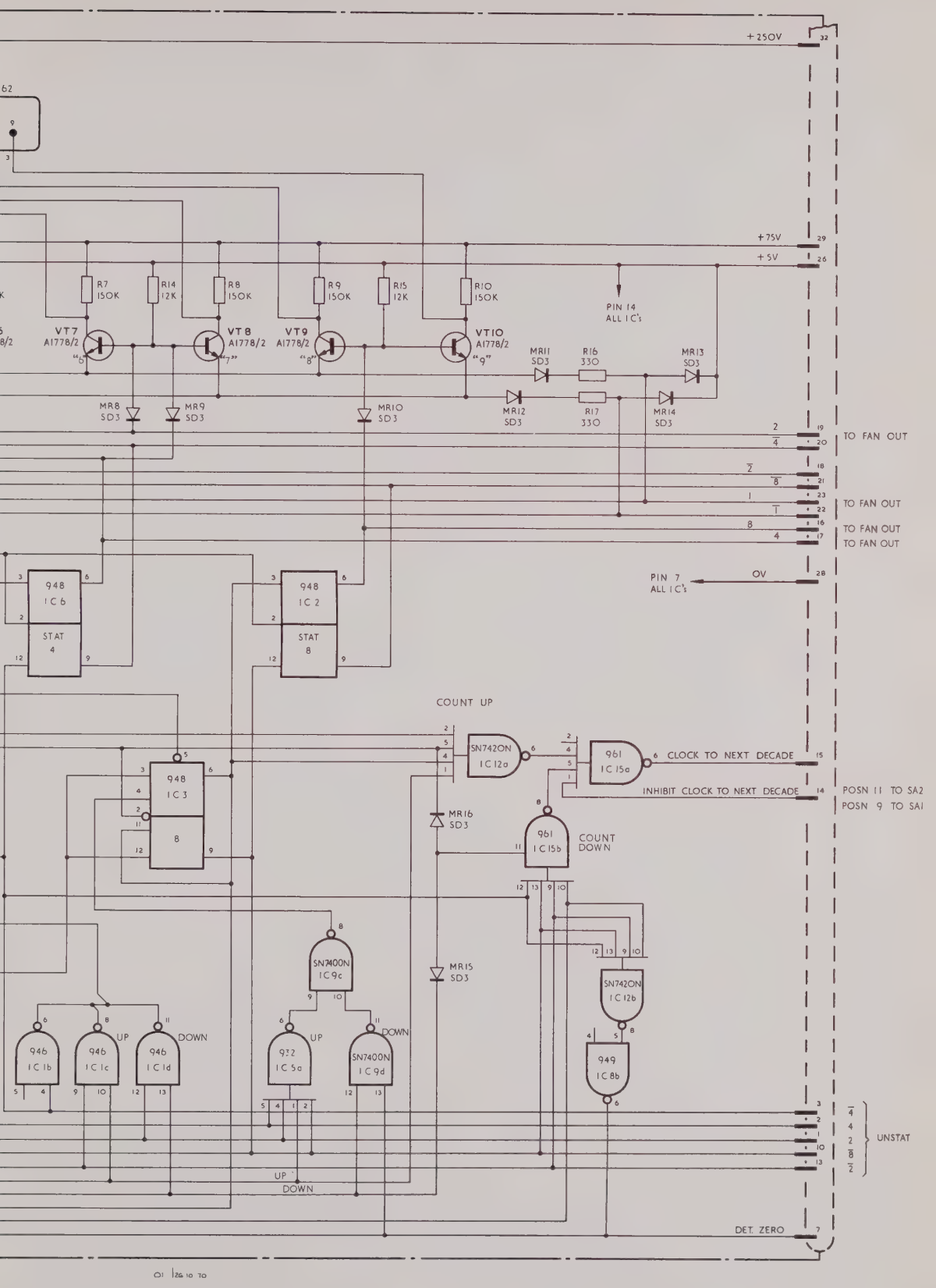
Cct. Ref.	General Description	Solartron Part No.
	Valve Base	300214020



RESET TABLE					BOARD POSN No
DECADE	IC14	IC11	IC7	C3	
UNITS	5	5	5	5	11
TENS	5	5	5	5	9
HUNDREDS	5	5	5	5	8
THOUSANDS	10	5	10	5	6
TEN THOUSANDS	10	5	10	5	4

NOTE –
CIRCUIT DRAWN AS FOR BOARD POSNS 8, 9 & 11. FOR POSNS 4 & 6 SEE TABLE.

PIN DESTINATIONS SHOWN AS POSN/PIN e.g. 3/15 INDICATES POSN 3 PIN 15
FOR DESTINATIONS NOT SHOWN SEE MOTHERBOARD CONNECTIONS



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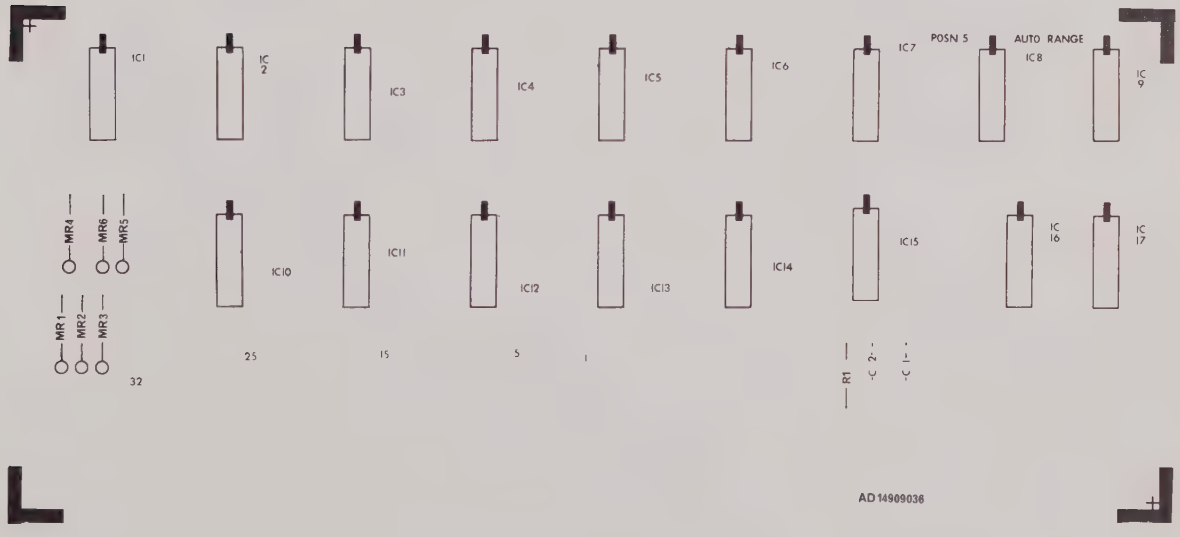
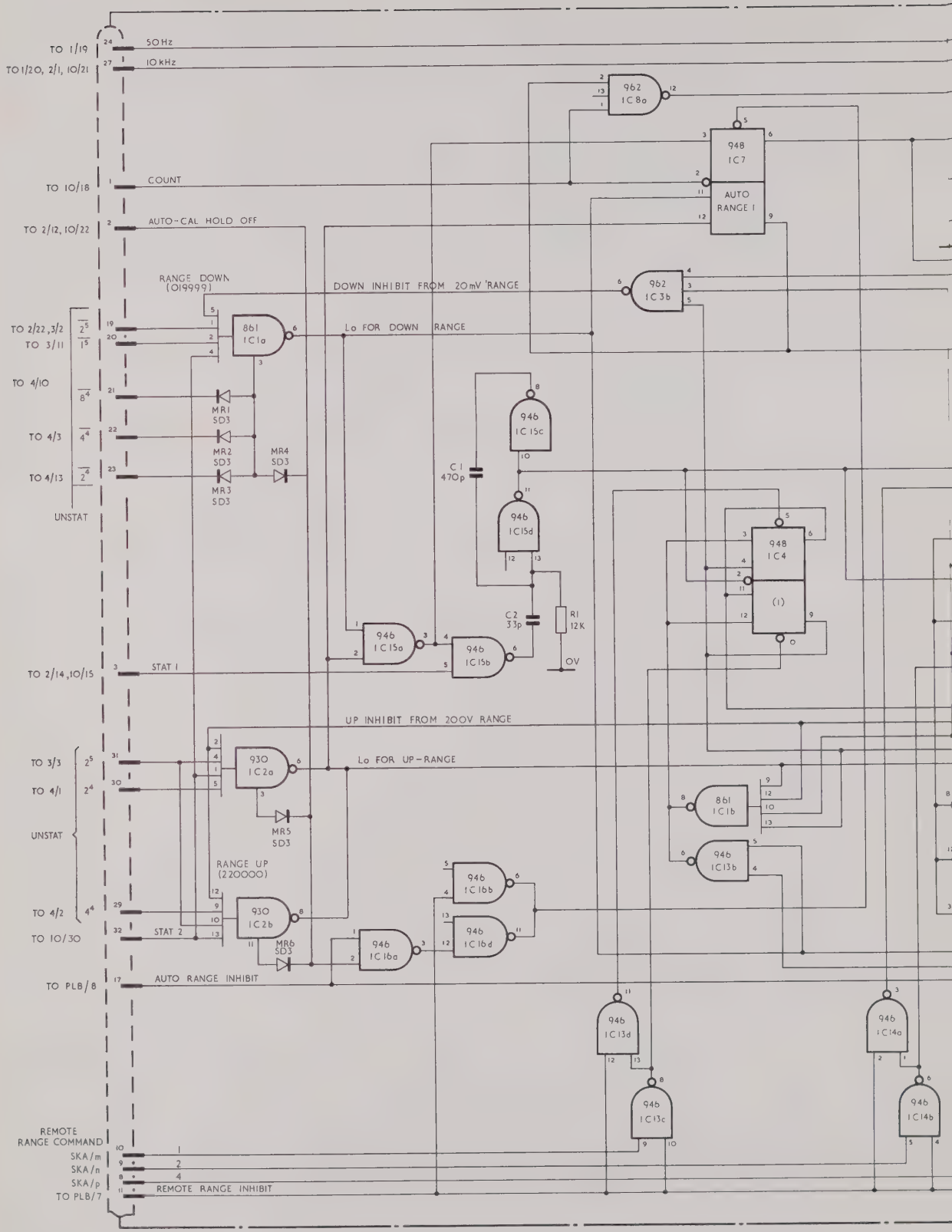
REVERSIBLE DECADE COUNTER. POSITIONS 4, 6, 8, 9 AND 11.

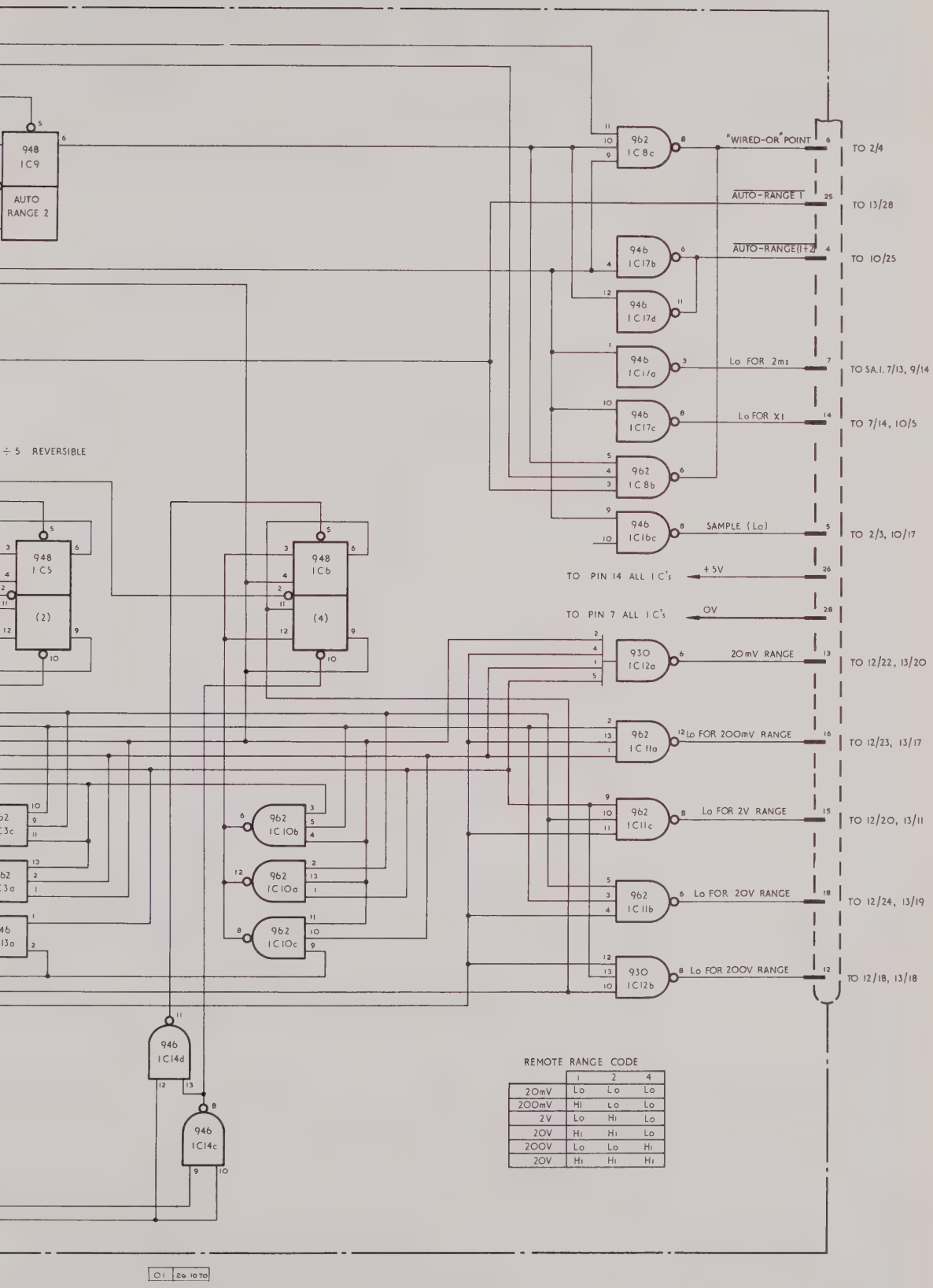
AUTO-RANGE P.C.B. (POSITION NO. 5)

Cct. Ref.	General Description		Solartron Part No.
MR1 to MR6	SD3	Solartron	300522160
IC1	IC930 Dual Four Input Gate		510000100
IC2	IC930 Dual Four Input Gate		510000100
IC3	IC962 Triple 3 Input Gate		510000200
IC4 to IC7	IC948 Clocked Flip-Flop		510000170
IC8	IC962 Triple 3 Input Gate		510000200
IC9	IC948 Clocked Flip-Flop		510000170
IC10	IC962 Triple 3 Input Gate		510000200
IC11	IC962 Triple 3 Input Gate		510000200
IC12	IC930 Dual Input Gate		510000100
IC13 to IC17	IC946 Quad 2 Input Gate		510000160
	Conn. Plug fixed 32 Way		352332040
R1	12k	½W 10%	17234200
C1	470p	500V 10%	208400084
C2	33p	750V 10%	208400088





NOTE
PIN DESTINATIONS SHOWN AS POS^{N}/PIN
e.g 3/15 INDICATES POS^{N} 3 PIN 15
FOR DESTINATIONS NOT SHOWN SEE
MOTHER BOARD CONNECTIONS

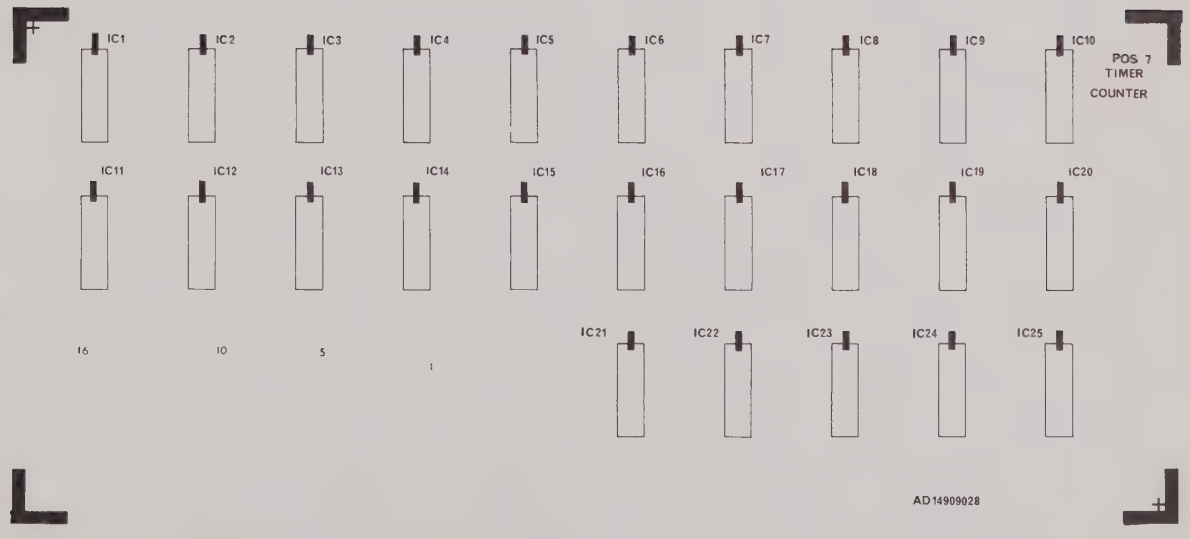


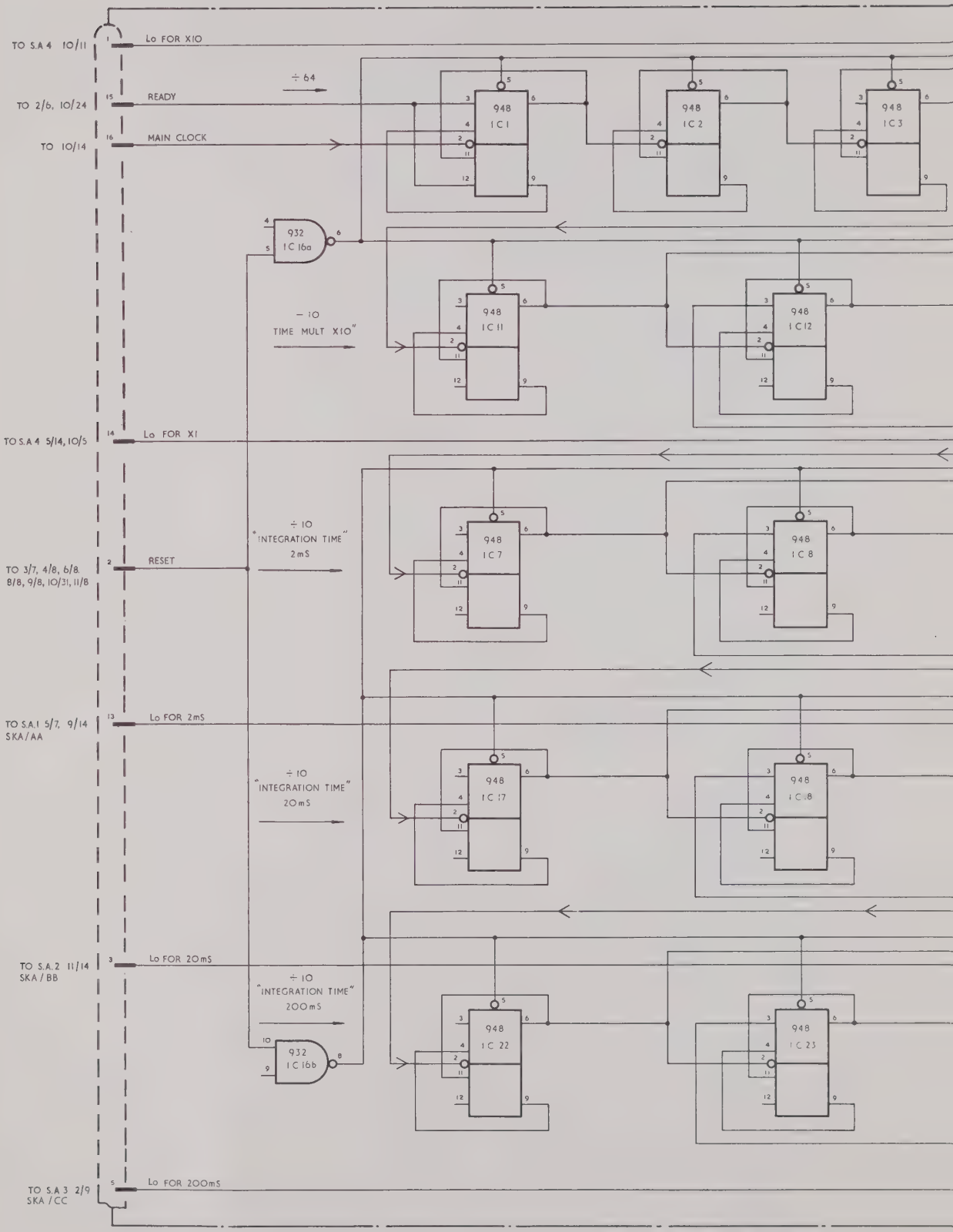
REMOTE RANGE CODE

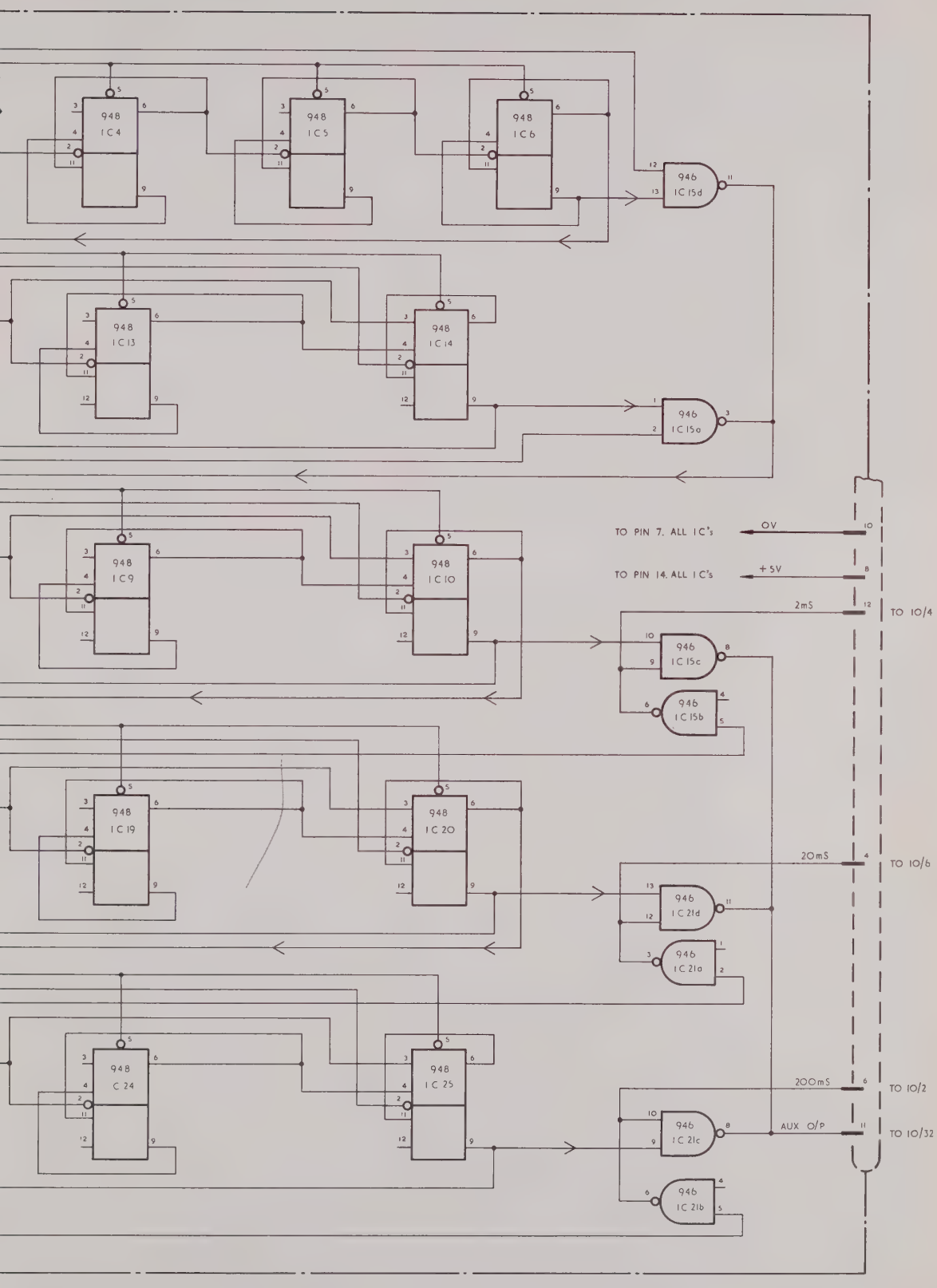
	1	2	4
20mV	Lo	Lo	Lo
200mV	Hi	Lo	Lo
2V	Lo	Hi	Lo
20V	Hi	Hi	Lo
200V	Lo	Lo	Hi
20V	Hi	Hi	Hi

TIME COUNTER P.C.B. (POSITION NO. 7)

Cct. Ref.	General Description	Solartron Part No.
IC1 to IC14	948 Clocked Flip-Flop	510000170
IC15	946 Quad 2 Input Gate	510000160
IC16	932 Dual Buffer	510000120
IC17 to IC20	948 Clocked Flip-Flop	510000170
IC21	946 Quad 2 Input Gate	510000160
IC22 to IC25	948 Clocked Flip-Flop	510000170




TO S.A 4 10/11
Lo FOR X10
÷ 64
TO 2/6, 10/24
READY
TO 10/14
MAIN CLOCK
948 IC1
948 IC2
948 IC3
932 IC 16a
948 IC 11
948 IC 12
÷ 10 TIME MULT X10"
TO S.A 4 5/14, 10/5
Lo FOR X1
÷ 10 "INTEGRATION TIME" 2mS
TO 3/7, 4/8, 6/8, 8/8, 9/8, 10/31, 11/8
RESET
948 IC 7
948 IC 8
TO S.A.1 5/7, 9/14 SKA/AA
Lo FOR 2mS
÷ 10 "INTEGRATION TIME" 20mS
948 IC 17
948 IC 18
TO S.A.2 11/14 SKA/BB
Lo FOR 20mS
÷ 10 "INTEGRATION TIME" 200mS
932 IC 16b
948 IC 22
948 IC 23
TO S.A 3 2/9 SKA/CC
Lo FOR 200mS

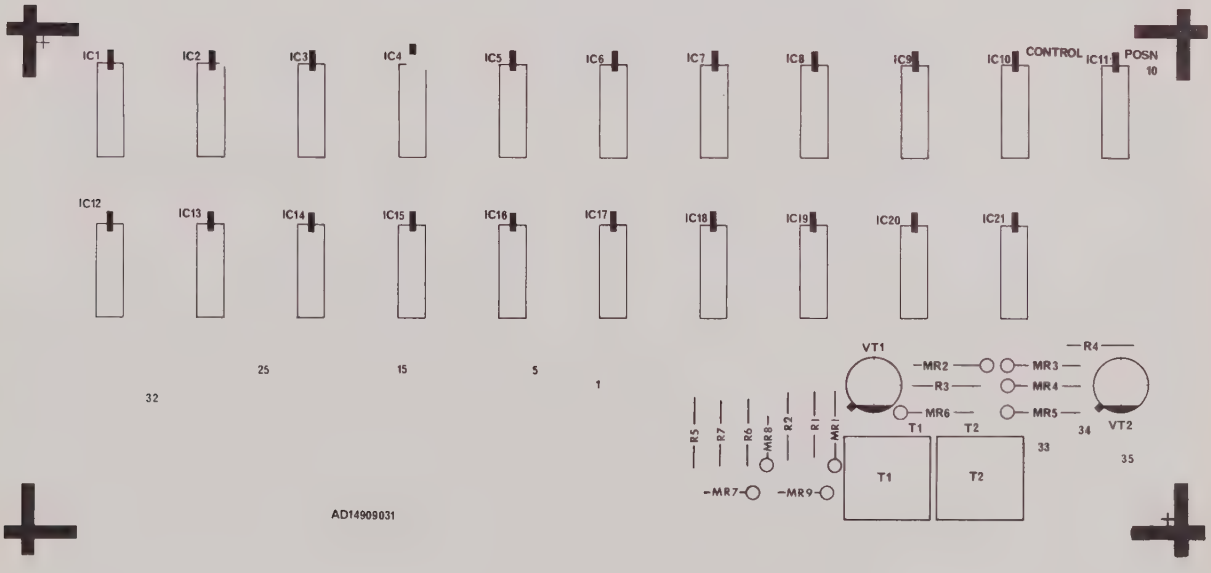

948 IC4
948 IC5
948 IC6
946 IC15d
948 IC13
948 IC14
946 IC15a
948 IC9
948 IC10
TO PIN 7. ALL IC's
0V
TO PIN 14. ALL IC's
+5V
2mS
TO 10/4
946 IC15c
946 IC15b
948 IC19
948 IC20
20mS
TO 10/6
946 IC21d
946 IC21a
948 C24
948 IC25
200mS
TO 10/2
946 IC21c
AUX O/P
TO 10/32
946 IC21b

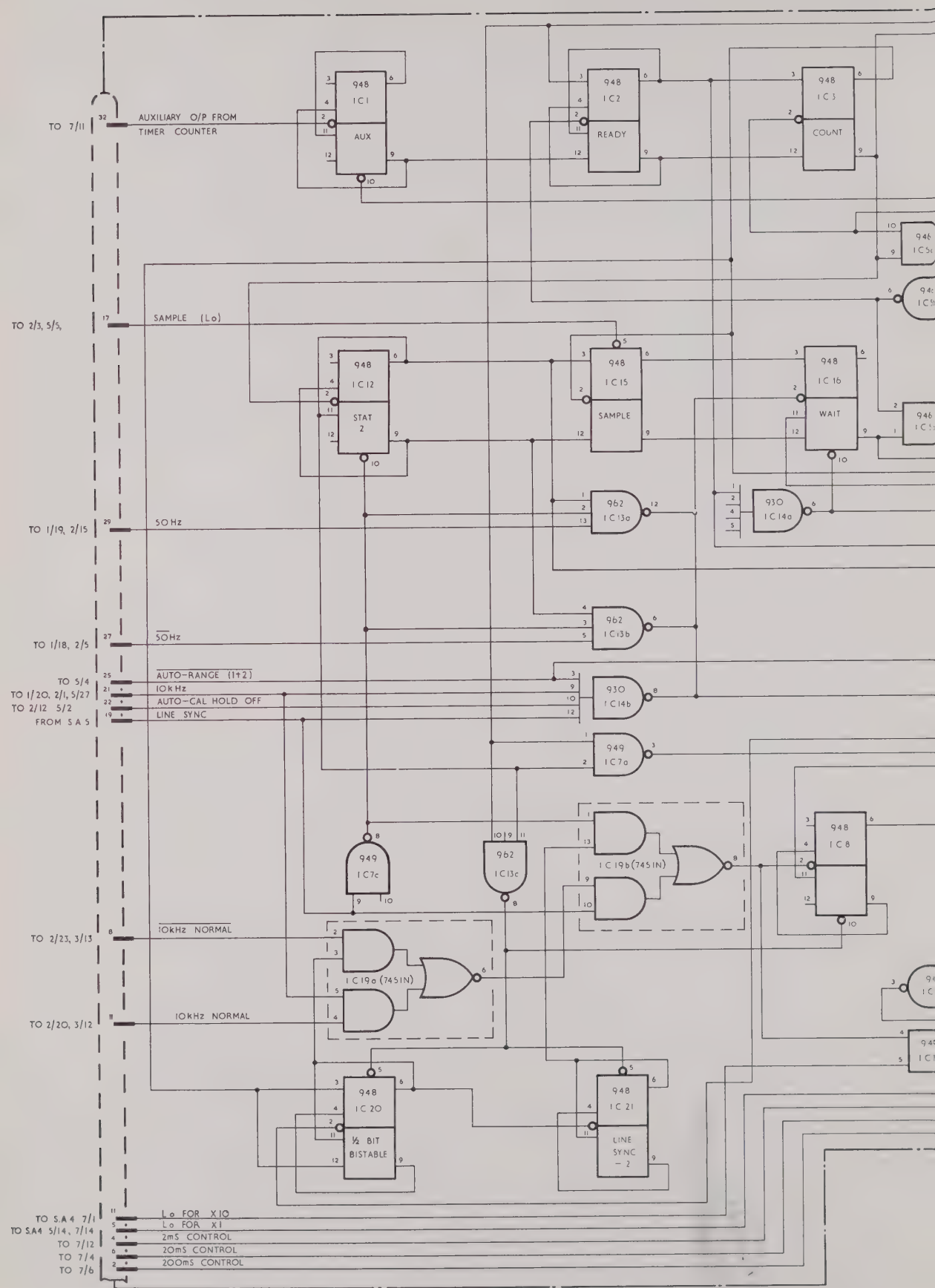
B 9-70

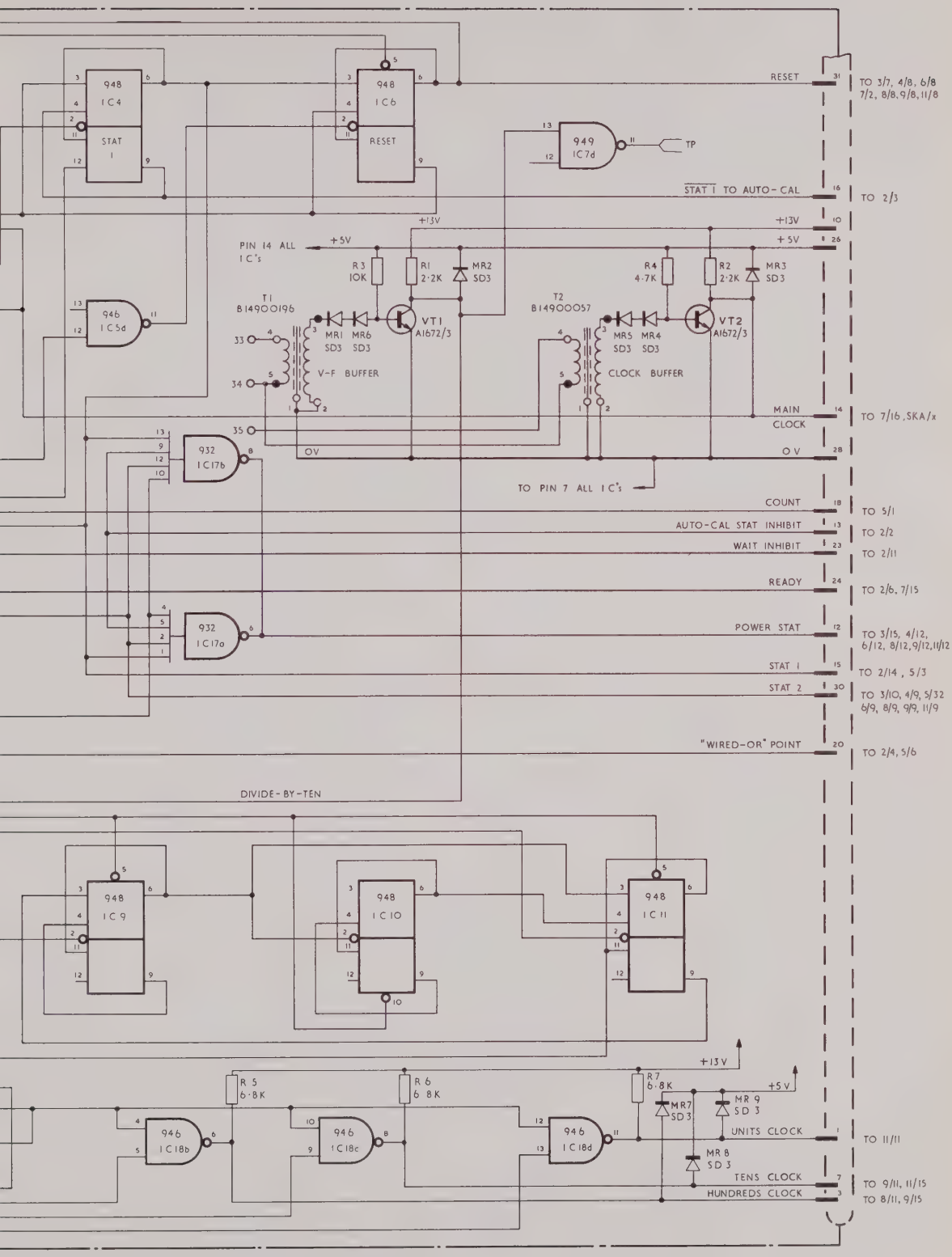
CONTROL LOGIC P.C.B. (POSITION NO. 10)

Cct. Ref.		General Description			Solartron Part No.
R1	X	2200	½W	10%	172332200
R2	X	2200	½W	10%	172332200
R3	X	10k	½W	10%	172341000
R4	X	4700	½W	10%	172334700
R5 to R7	X	6.8k	¼W	10%	172326800
MR1 to MR9		SD3			300522160
VT1		A1672/3			300551910
VT2		A1672/3			300551910
IC1 to IC4		948 Clocked Flip-Flop			510000170

Cct. Ref.	General Description	Solartron Part No.
IC5	946 Quad 2 Input Gate	510000160
IC6	948 Clocked Flip-Flop	510000170
IC7	849 Quad 2 Input Gate	510000370
IC8 to IC12	948 Clocked Flip-Flop	510000170
IC13	962 Tripple 3 Input Gate	510000200
IC14	930 Dual Four Input Gate	510000100
IC15	948 Clocked Flip-Flop	510000170
IC16	948 Clocked Flip-Flop	510000170
IC17	932 Dual Buffer	510000120
IC18	846 Quad 2 Input Gate	510000160
IC19	745IN Dual Exclusive or Gate	510000210
IC20	948 Clocked Flip-Flop	510000170
IC21	948 Clocked Flip-Flop	510000170
T1	Transformer	B14900196
T2	Transformer	B14900057




TO 7/11
AUXILIARY O/P FROM TIMER COUNTER
948 IC1 AUX
948 IC2 READY
948 IC3 COUNT
TO 2/3, 5/5,
SAMPLE (Lo)
948 IC12 STAT 2
948 IC15 SAMPLE
948 IC16 WAIT
TO 1/19, 2/15
50Hz
962 IC13a
930 IC14a
TO 1/18, 2/5
50Hz
962 IC13b
TO 5/4
AUTO-RANGE (1+2)
TO 1/20, 2/1, 5/27
10kHz
TO 2/12 5/2
AUTO-CAL HOLD OFF
FROM S A 5
LINE SYNC
930 IC14b
949 IC7a
949 IC7c
962 IC13c
IC19b (74S1N)
948 IC8
TO 2/23, 3/13
10kHz NORMAL
IC19a (74S1N)
TO 2/20, 3/12
10kHz NORMAL
948 IC20 ½ BIT BISTABLE
948 IC21 LINE SYNC ÷ 2
TO S.A 4 7/1
Lo FOR X10
TO S.A4 5/14, 7/14
Lo FOR X1
TO 7/12
2mS CONTROL
TO 7/4
20mS CONTROL
TO 7/6
200mS CONTROL



TINATIONS SHOWN AS POS^N/PIN
INDICATES POS^N 3 PIN 15

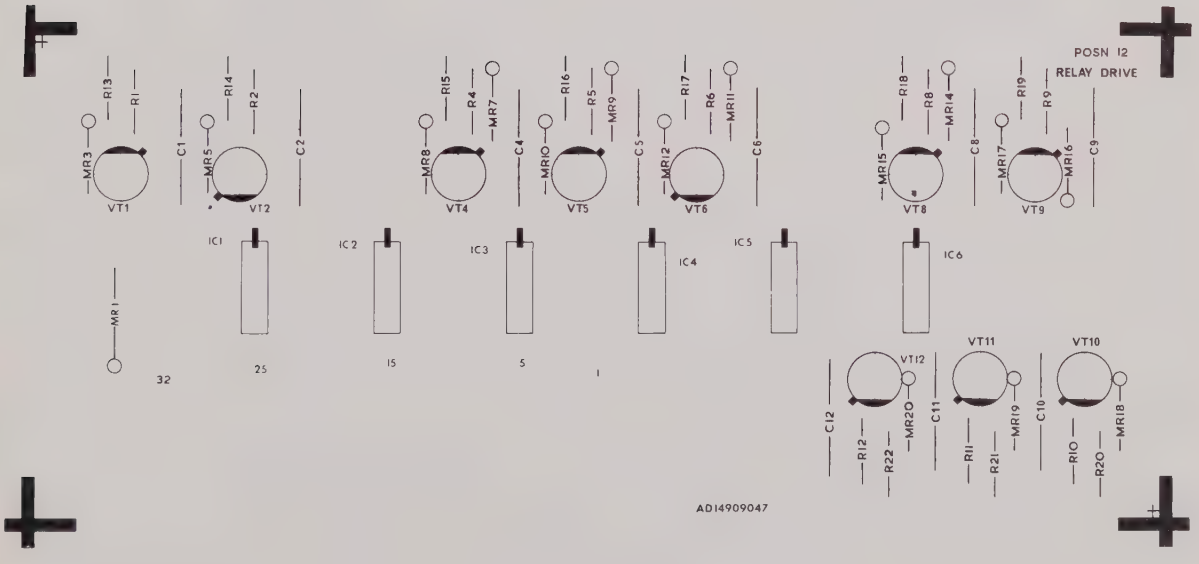
FOR DESTINATIONS NOT SHOWN SEE MOTHER BOARD CONNECTIONS

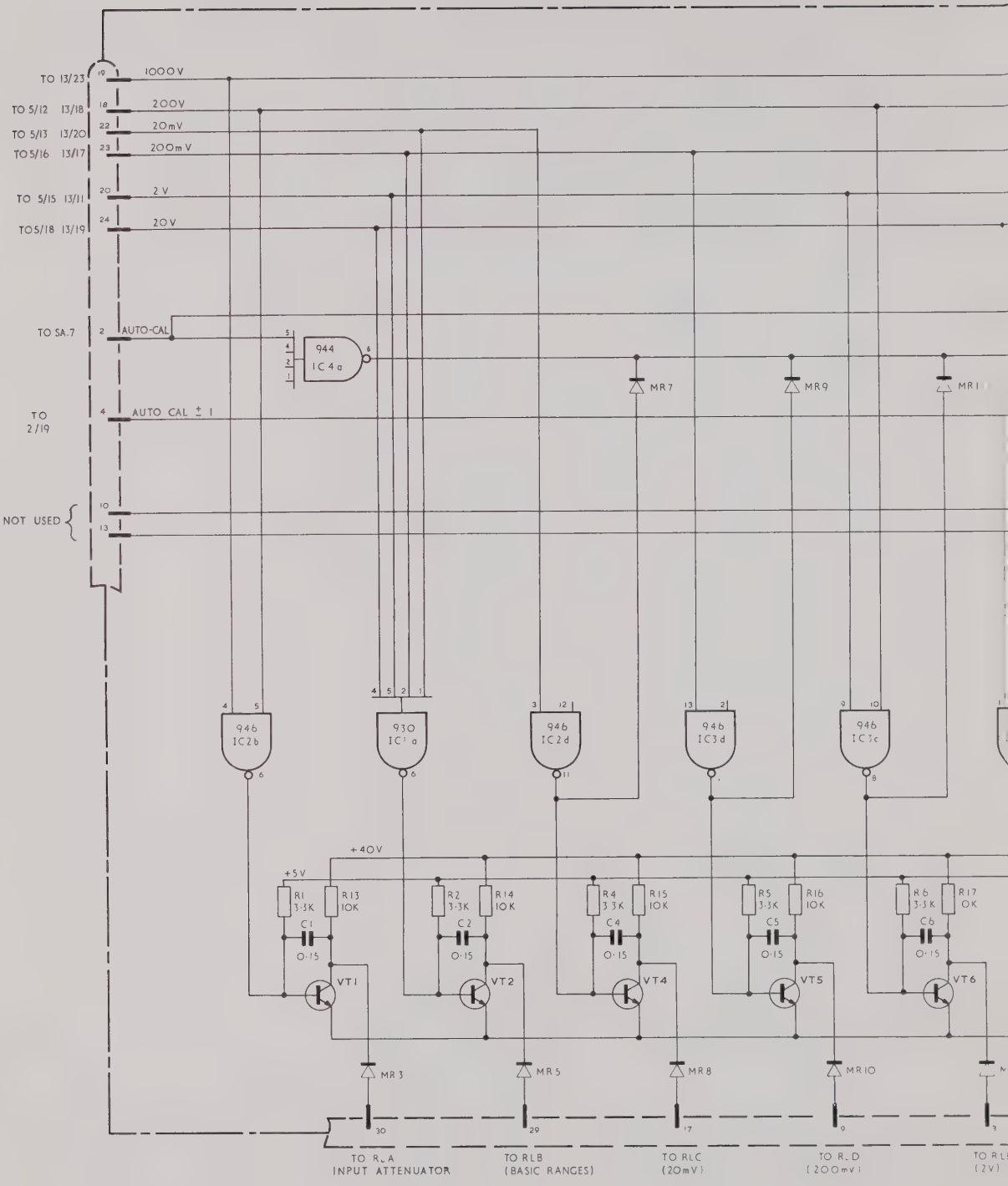
D1 |26-10-70

RELAY DRIVE P.C.B. (POSITION NO. 12)

Cct. Ref.		General Description			Solartron Part No.
R1	X	3300	½W	10%	172333300
R2	X	3300	½W	10%	172333300
R4 to R6	X	3300	½W	10%	172333300
R8 to R12	X	3300	½W	10%	172333300
R13 to R22	X	10k	½W	10%	172341000
C1		0.15	160V	10%	220351500
C2		0.15	160V	10%	220351500
C4 to C6		0.15	160V	10%	220351500
C8 to C12		0.15	160V	10%	220351500

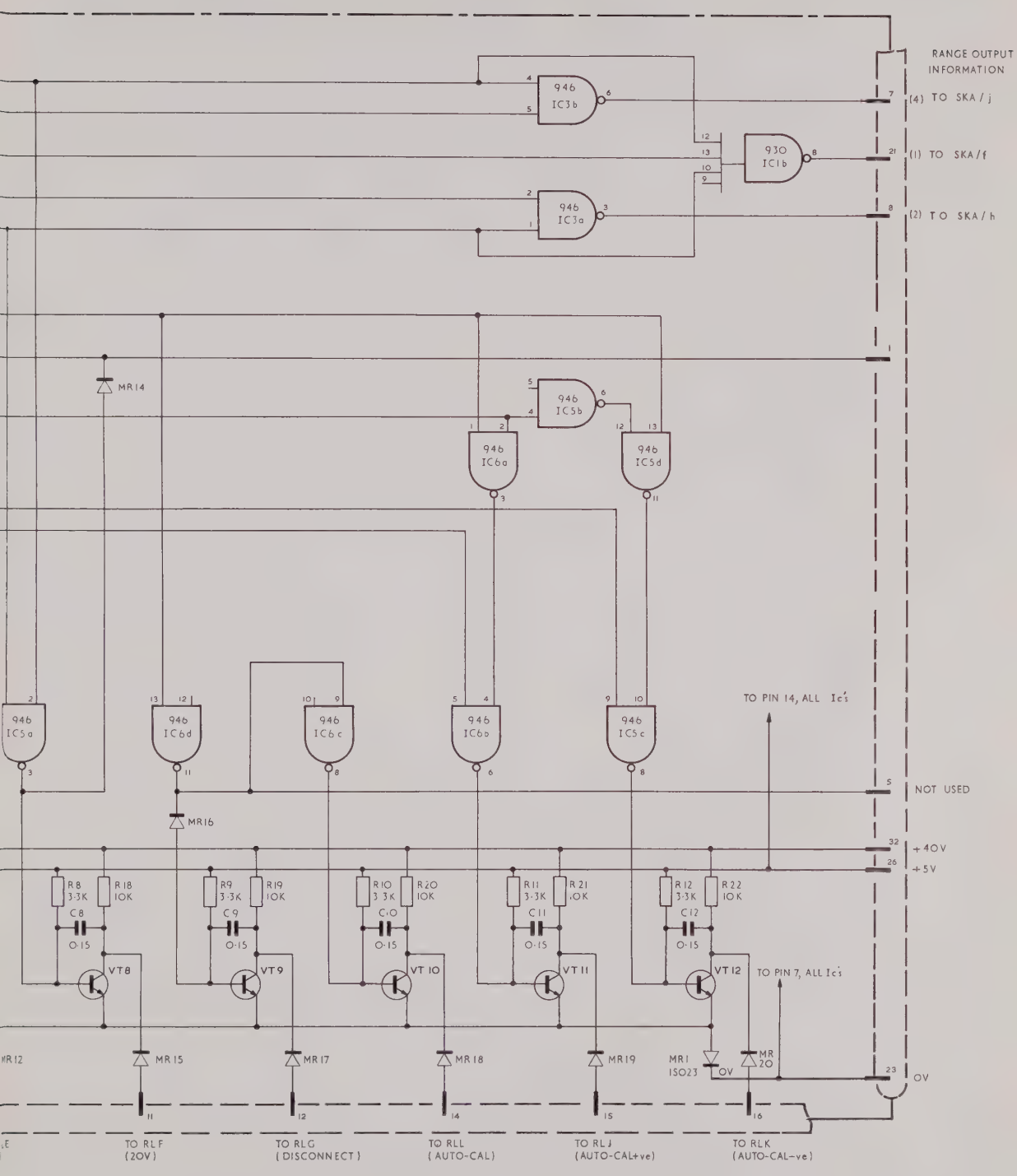
Cct. Ref.	General Description	Solartron Part No.
MR1	IS023	300524200
MR3	SD3	300522160
MR5	SD3	300522160
MR7 to MR12	SD3	300522160
MR14 to MR20	SD3	300522160
VT1	BSX51A	300552960
VT2	BSX51A	300552960
VT4	BSX51A	300552960
VT5	BSX51A	300552960
VT6	BSX51A	300552960
VT8 to VT12	BSX51A	300552960
IC1	IC930 Dual 4 Input Gate	510000100
IC2	IC946 Quad 2 Input Gate	510000160
IC3	IC946 Quad 2 Input Gate	510000160
IC4	IC944 Dual 4 Input Power Gate	510000140
IC5	IC946 Quad 2 Input Gate	510000160
IC6	IC946 Quad 2 Input Gate	510000160





NOTES

1 ALL DIODES TO BE SD3, UNLESS OTHERWISE STATED
2 ALL TRANSISTORS TO BE BSX51A
3 PIN DESTINATIONS SHOWN AS POSN/PIN
eg 2/19 INDICATES POSN/PIN 19


RANGE OUTPUT INFORMATION
946 IC3b
930 IC1b
946 IC3a
(4) TO SKA/j
(1) TO SKA/f
(2) TO SKA/h
MR14
946 IC5b
946 IC6a
946 IC5d
946 IC5a
946 IC6d
946 IC6c
946 IC6b
946 IC5c
TO PIN 14, ALL Ic's
NOT USED
MR16
+40V
+5V
R8 3·3K
R18 10K
C8 0·15
R9 3·3K
R19 10K
C9 0·15
R10 3·3K
R20 10K
C10 0·15
R11 3·3K
R21 10K
C11 0·15
R12 3·3K
R22 10K
C12 0·15
VT8
VT9
VT10
VT11
VT12
TO PIN 7, ALL Ic's
MR15
MR17
MR18
MR19
MR1 ISO23
MR 20
0V
0V
TO RLF (20V)
TO RLG (DISCONNECT)
TO RLL (AUTO-CAL)
TO RLJ (AUTO-CAL+ve)
TO RLK (AUTO-CAL-ve)

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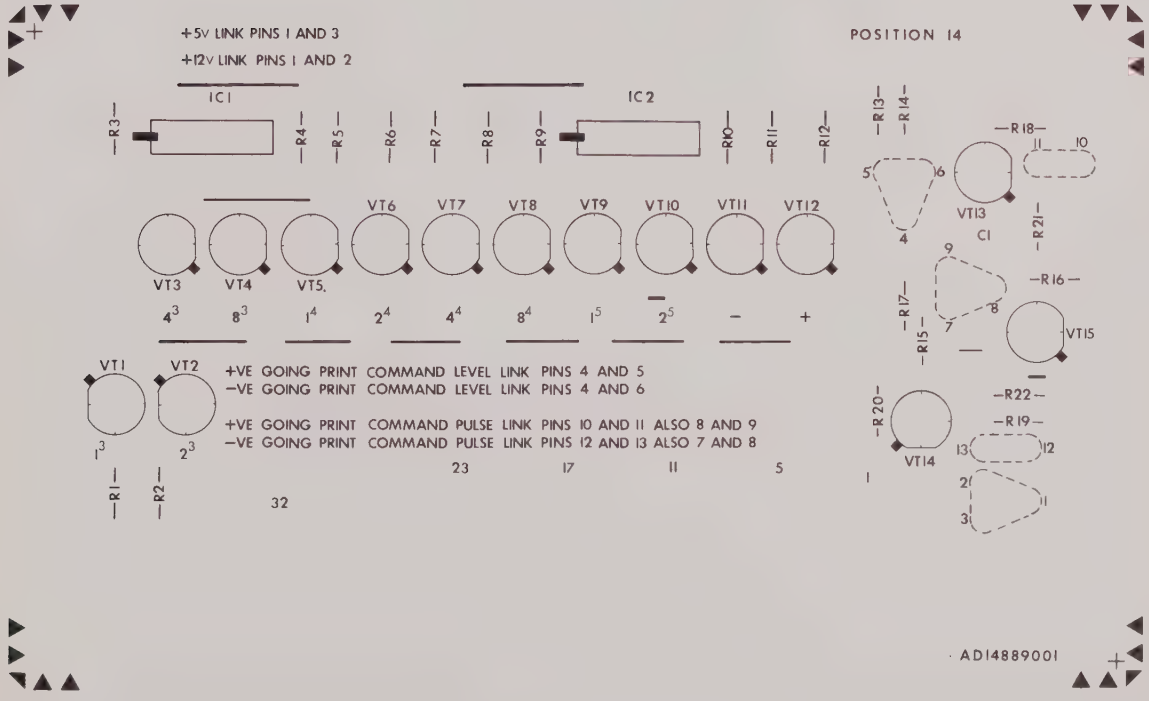
POSITIVE LOGIC FAN OUT EX1488 POSITION 14

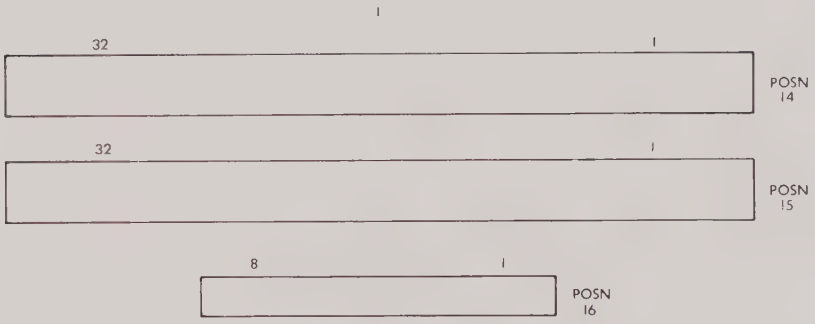
Cct. Ref.		General Description			Solartron Part No.
R1 to R14	X	1.5k	1/8W	10%	172031500
R15	X	12k	1/8W	10%	172041200
R16	X	1.5k	1/8W	10%	172031500
R17	X	4.7k	1/8W	10%	172034700
R18	X	4.7k	1/8W	10%	172034700
R19	X	10k	1/8W	10%	172041000
R20	X	4.7k	1/8W	10%	172034700
R21	X	10k	1/8W	10%	172041000
R22	X	4.7k	1/8W	10%	172034700

Cct. Ref.		General Description			Solartron Part No.
C1	G	.001	500V	± 20%	241331000
VT1 to VT12		BC107			300553320
VT13 to VT15		A1672/3			300551910
IC1		Hex Inverter SN15836N			510000290
IC2		Hex Inverter SN15836N			510000290
		Conn. Plug 32 Way			352332040



FAN-OUT MOTHER BOARD

Cct. Ref.	General Description	Solartron Part No.
	Conn. Socket 8 Way	352508040
	Conn. Socket 32 Way	352532220

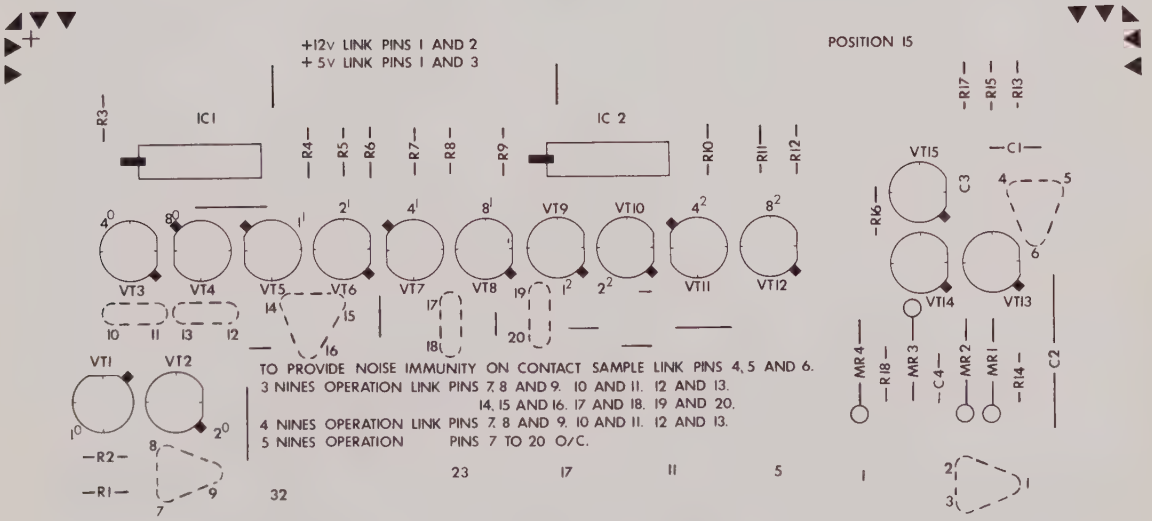


AD/4909043

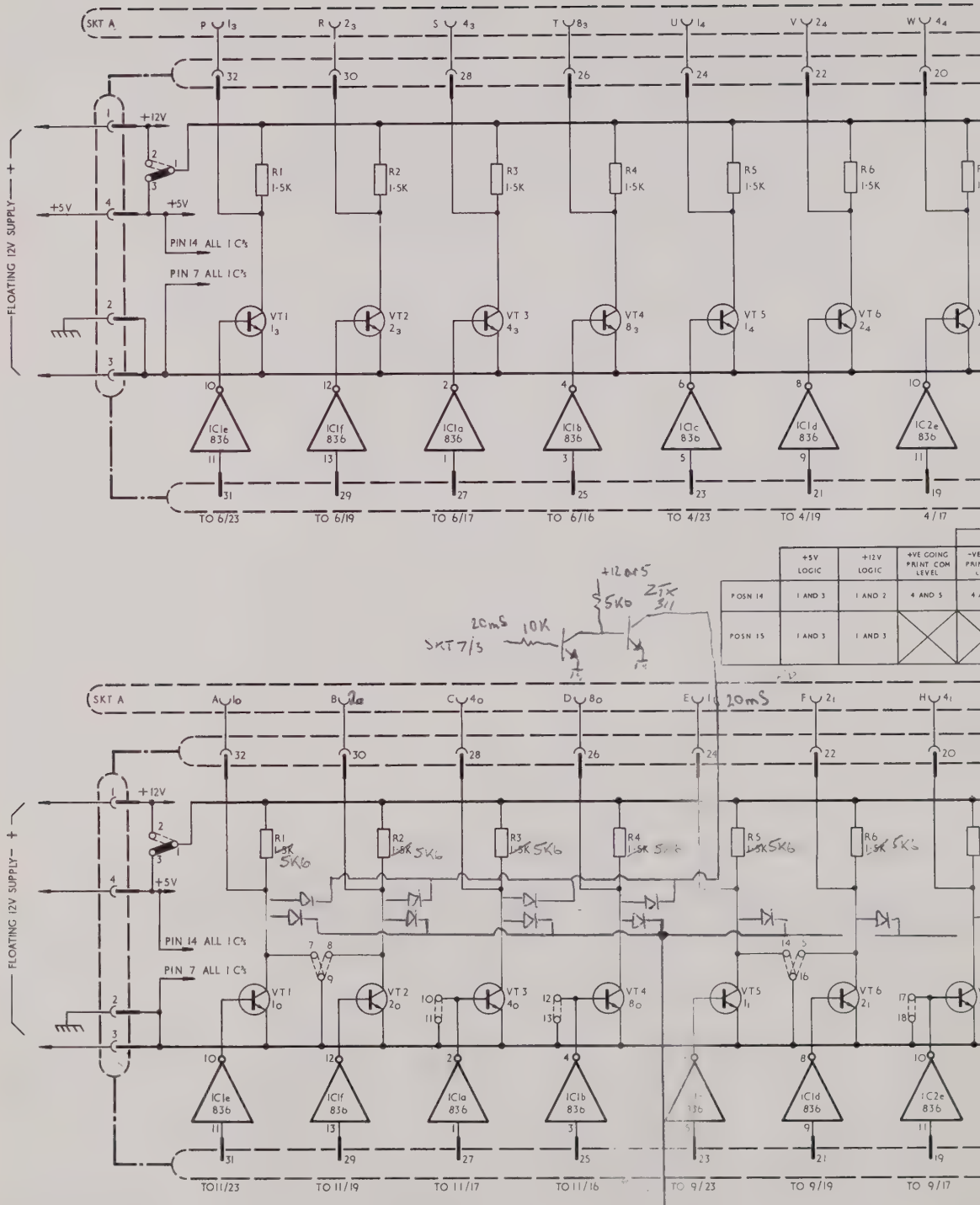
POSITIVE LOGIC FAN OUT EX1488 POSITION 15

Cct. Ref.		General Description			Solartron Part No.
R1 to R12	X	1.5k	1/8W	10%	172031500
R13	X	39k	1/8W	10%	172043900
R14	X	1k	1/8W	10%	172031000
R15	X	4.7k	1/8W	10%	172034700
R16	X	10k	1/8W	10%	172041000
R17	X	3.3k	1/8W	10%	172033300
R18	X	1.8k	1/8W	10%	172031800
C1	B	.1	100V	20%	225451000
C2	B	1	63V	20%	219961000
C3	G	2200p	500V	20%	241332200
C4	B	.1	100V	20%	225451000

Cct. Ref.	General Description	Solartron Part No.
MR1 to MR4	Diode SD3	300522160
VT1 to VT13	BC107	300553320
VT14	SM6526	300552990
VT15	BC107	300553320
IC1	Hex Inverter SN15836N	510000290
IC2	Hex Inverter SN15836N	510000290
	Conn. Plug 32 Way	352332040



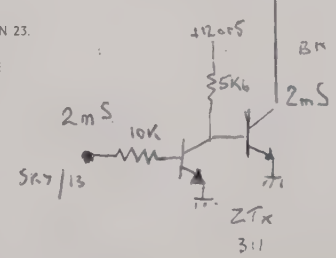
AD 14889002

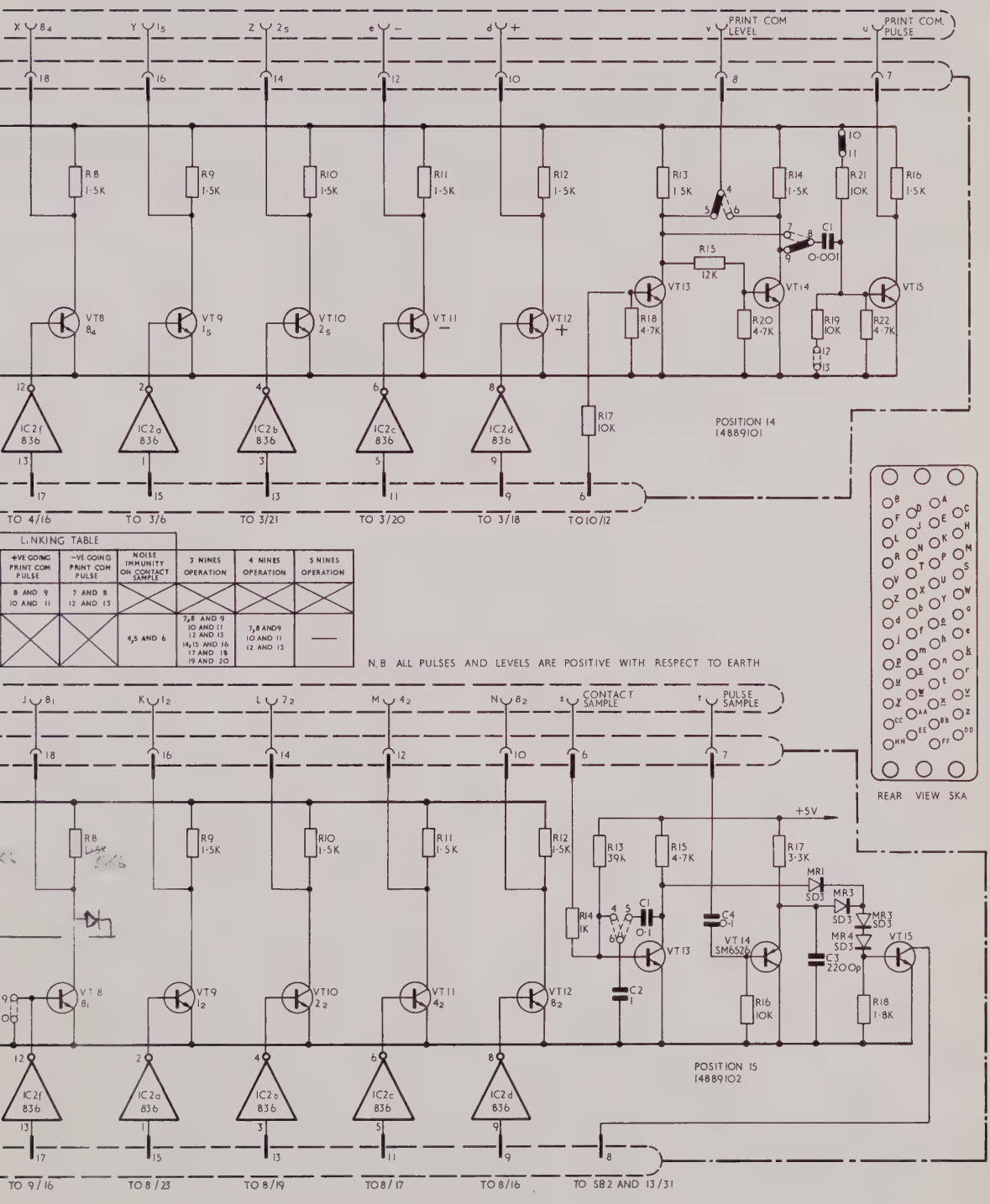


	+5V LOGIC	+12V LOGIC	+VE GOING PRINT COM LEVEL	-VE PRIN
POSN 14	1 AND 3	1 AND 2	4 AND 5	4 A
POSN 15	1 AND 3	1 AND 3		

NOTE:-

1. ALL PIN DESTINATIONS SHOWN AS POSN/PIN e.g. 11/23 POSN 11 PIN 23.
2. UNLESS OTHERWISE STATED ALL TRANSISTORS ARE BC107/S.
3. CIRCUIT SHOWS STANDARD LINKS FITTED FOR +5V LOGIC AND +VE GOING PRINT COMMAND PULSE AND LEVEL.



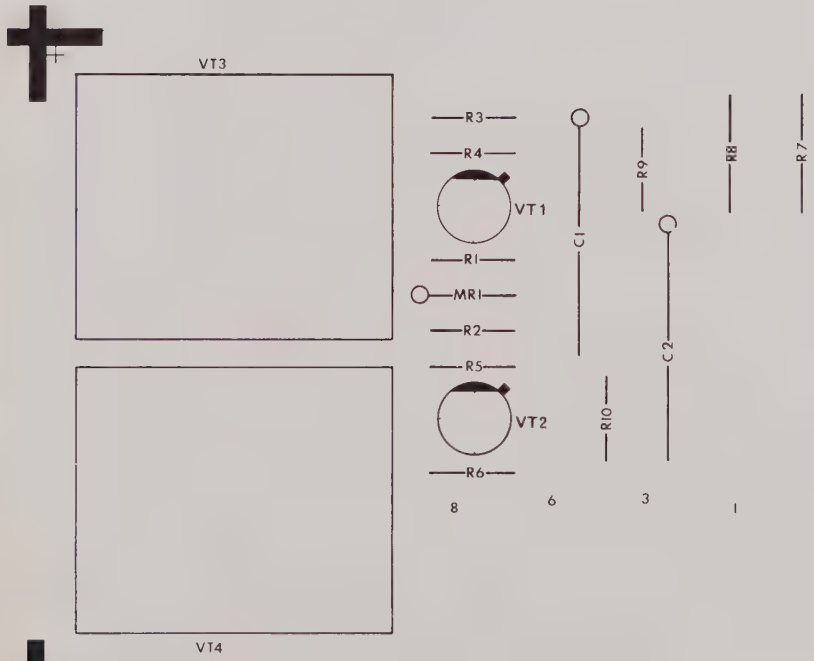

X 8₄
Y 1₅
Z 2₅
e –
d +
v PRINT COM LEVEL
u PRINT COM. PULSE
R8 1·5K
R9 1·5K
R10 1·5K
R11 1·5K
R12 1·5K
R13 1·5K
R14 1·5K
R21 10K
R16 1·5K
C1 0·001
R15 12K
VT8 8₄
VT9 1₅
VT10 2₅
VT11 –
VT12 +
VT13
VT14
VT15
R18 4·7K
R20 4·7K
R19 10K
R22 4·7K
IC2f 836
IC2a 836
IC2b 836
IC2c 836
IC2d 836
R17 10K
POSITION 14
14889101
TO 4/16
TO 3/6
TO 3/21
TO 3/20
TO 3/18
TO 10/12
LINKING TABLE
+VE GOING PRINT COM PULSE
–VE GOING PRINT COM PULSE
NOISE IMMUNITY ON CONTACT SAMPLE
3 NINES OPERATION
4 NINES OPERATION
5 NINES OPERATION
8 AND 9 10 AND 11
7 AND 8 12 AND 13
4,5 AND 6
7,8 AND 9 10 AND 11 12 AND 13 14,15 AND 16 17 AND 18 19 AND 20
3,8 AND 9 10 AND 11 12 AND 13
N.B ALL PULSES AND LEVELS ARE POSITIVE WITH RESPECT TO EARTH
REAR VIEW SKA
J 8₁
K 1₂
L 2₂
M 4₂
N 8₂
s CONTACT SAMPLE
t PULSE SAMPLE
+5V
R13 39k
R15 4·7K
R17 3·3K
MR1 SD3
MR3 SD3
MR4 SD3
R14 1K
C1 0·1
C4 0·1
VT13
VT14 SM6526
VT15
C2 1
C3 2200p
R16 10K
R18 1·8K
POSITION 15
14889102
TO 9/16
TO 8/23
TO 8/19
TO 8/17
TO 8/16
TO SB2 AND 13/31

1·9·70| 01

FLUX OSCILLATOR P.C.B. (POSITION NO. 16)

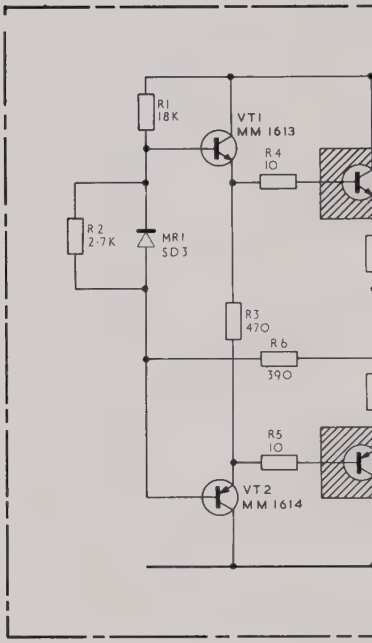
Cct. Ref.		General Description			Solartron Part No.
R1	X	18k	½W	10%	172341800
R2	X	2700	½W	10%	172332700
R3	X	470	½W	10%	172324700
R4	X	10	½W	10%	172311000
R5	X	10	½W	10%	172311000
R6	Z	390	½W	5%	193523900
R7	Y	3.3	2.6W	5%	173403300
R8	Y	3.3	2.6W	5%	173403300
R9	X	2200	½W	10%	172332200
R10	X	2200	½W	10%	172332200

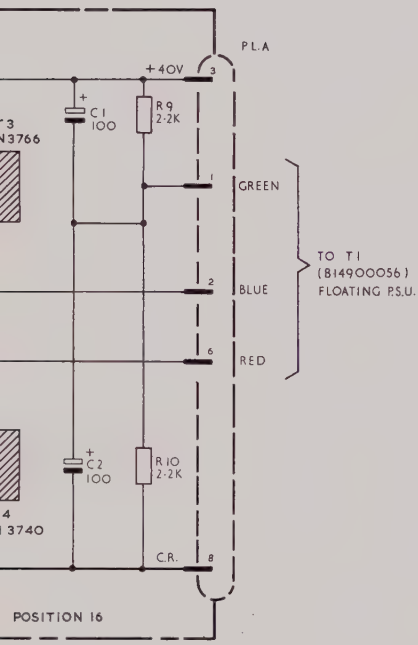
Cct. Ref.	General Description			Solartron Part No.
C1	100	25V	−20% +100%	260781003
C2	100	25V	−20% +100%	260781003
MR1	SD3			300522160
VT1	MM1613			300552000
VT2	MM1614			300551670
VT3	2N3766			300553250
VT4	2N3740			300553270



POSN 16
FLUX OSCILLATOR

AD 14909045

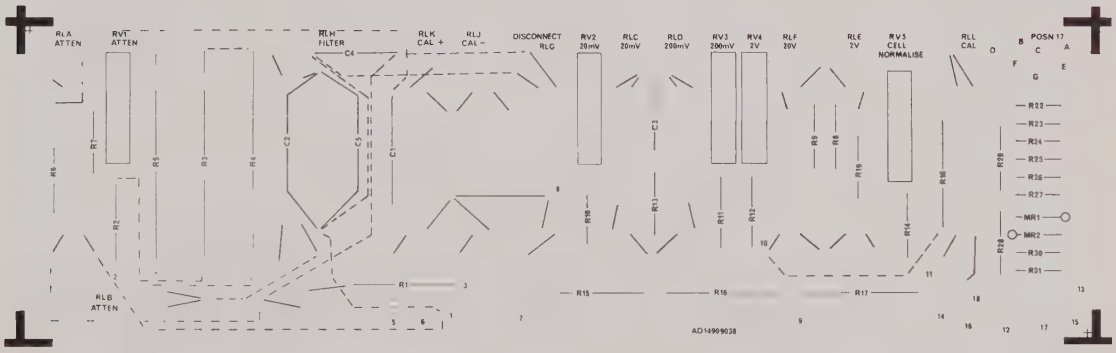

R1
18K
VT1
MM 1613
R4
10
R2
2·7K
MR1
SD3
R3
470
R6
390
R5
10
VT2
MM 1614

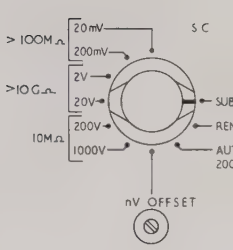

P.L.A
+40V
3
C1
100
R9
2·2K
T3
N3766
1
GREEN
TO T1
(B14900056)
FLOATING P.S.U.
2
BLUE
6
RED
C2
100
R10
2·2K
4
3740
C.R.
8
POSITION 16

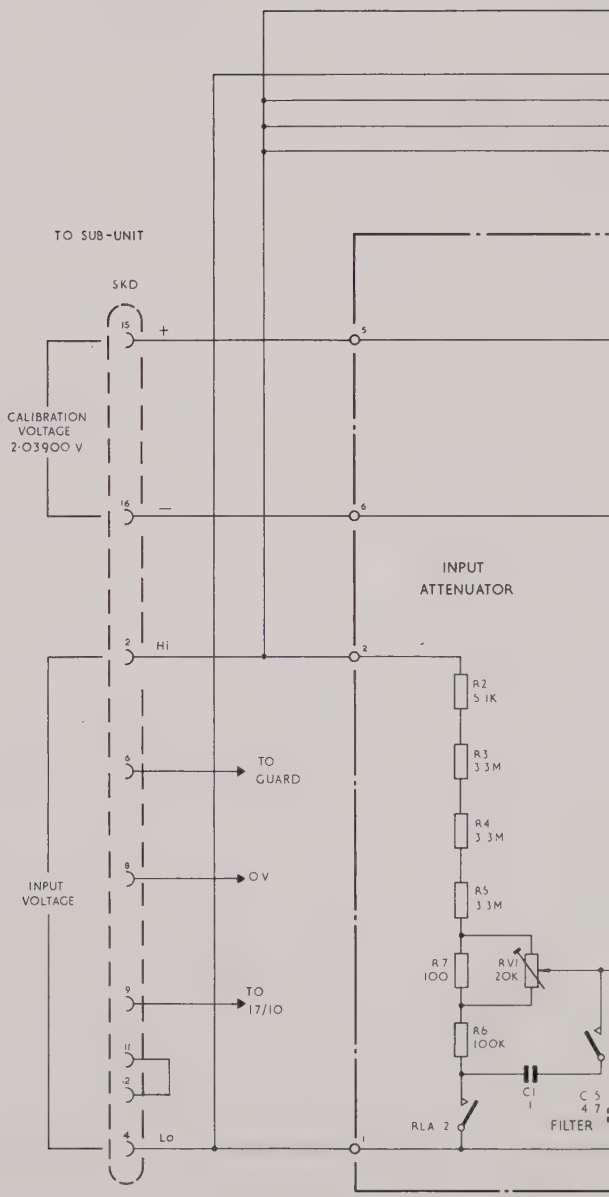
F 10·9·69

INPUT SWITCHING P.C.B. (POSITION NO. 17)

Cct. Ref.		General Description			Solartron Part No.
R1	V	10k	1W	1%	
R2	V	5100	¼W	1%	
R3		3.3M	To spec		198741001
R4		3.3M	To spec		198335102
R5		3.3M	To spec		B14900044
R6		100k	To spec		
R7	V	100	¼W	1%	198321002
R8	V	10k	¼W	1%	198341002
R9	V	300k	¼W	1%	198353002
R10	V	30k	¼W	1%	198343002
R11		120k	1/8W	0.5%	B14900303
R12		400k	1/8W	0.25%	B14900303
R13	W	1200	¼W	1%	170431200
R14		190	¼W	0.5%	B14900303
R15		100.25	To spec		B14900045
R16		906.3	To spec		
R17		9202	To spec		
R18		89.8k	To spec		
R19		10	¼W	1%	B14900303
R22	Z	2200	½W	5%	193532200
R23	Z	2200	½W	5%	193532200
R24	Z	2200	½W	5%	193532200
R25	Z	2200	½W	5%	193532200
R26	Z	2200	½W	5%	193532200
R27	Z	2200	½W	5%	193532200
R28	W	1.5M	¼W	5%	170561500
R29	Z	470k	½W	5%	193554700
R30	Z	3300	½W	5%	193533300
R31	Z	3300	½W	5%	193533300
RV1 to RV4		20k	¼W	10%	122042000
RV5		5000	¼W	10%	122035000
C1		1.0	160V	10%	220361000
C2		4.7	100V	10%	219864700
C3		0.1	100V	20%	208200055
C4		0.01	63V	10%	209941000
C5		4.7	100V	10%	219864700
MR1		SZD5.6			300521450
MR2		SZD5.6			300521450
RLA to RLH		Relay			AD16370050
RLJ to RLL		Relay			





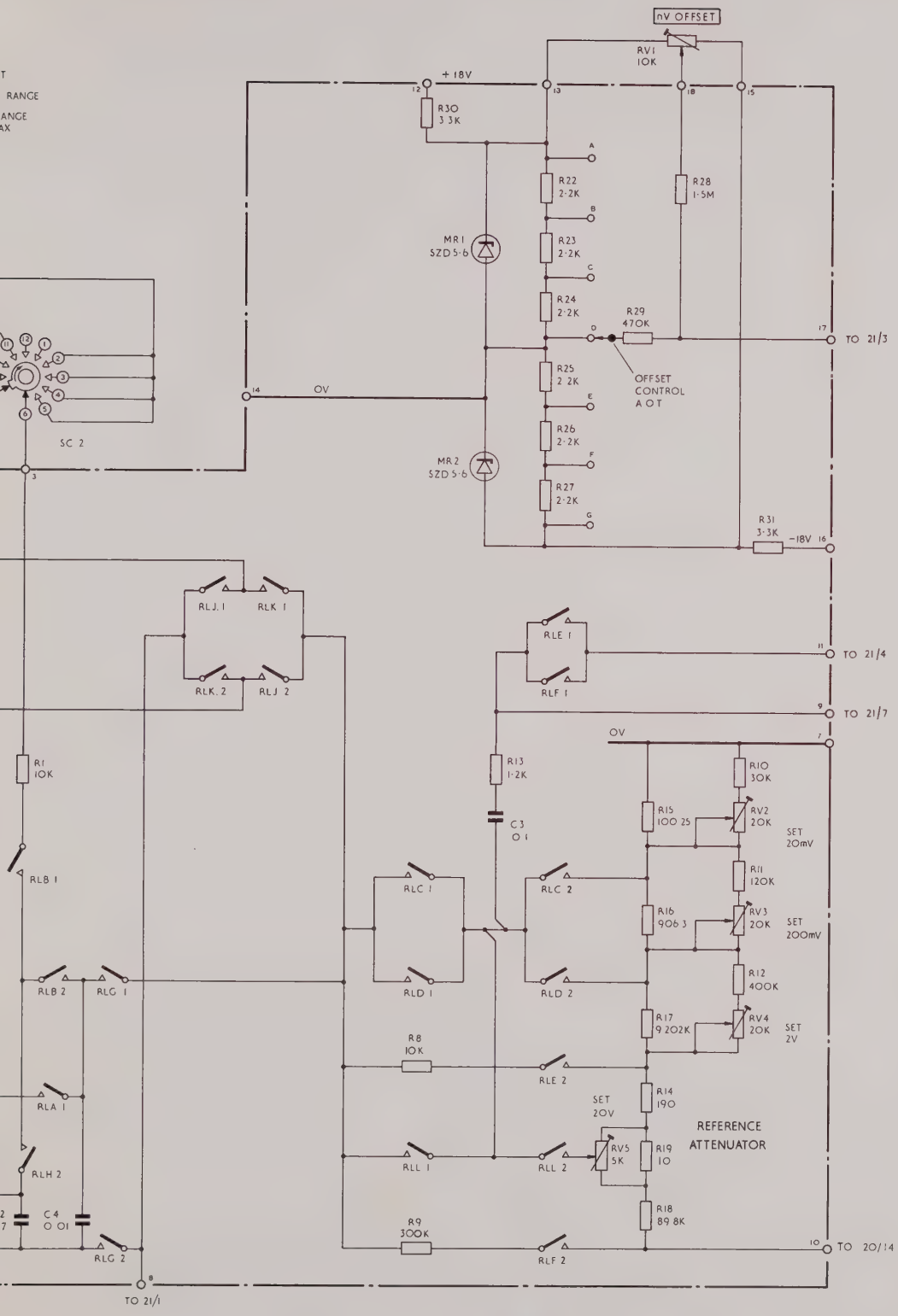


RELAY CHART

RELAY CCT REF	FUNCTION
RLA	INPUT ATTENUATOR
RLB	BASIC RANGES
RLC	20mV RANGE
RLD	200mV RANGE
RLE	2V RANGE
RLF	20V RANGE
RLG	AUTO-CAL INPUT DISCONNECT
RLH	FILTER
RLJ	AUTO-CAL −
RLK	AUTO-CAL +
RLL	AUTO-CAL RANGE

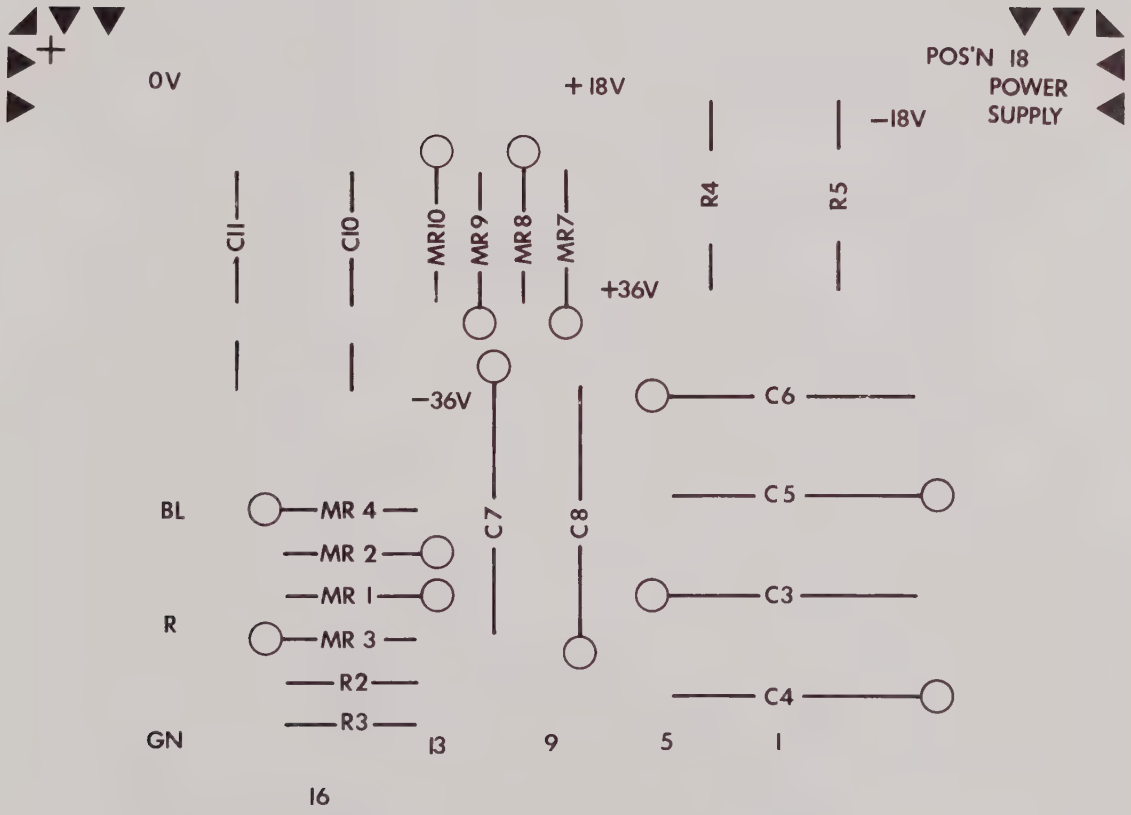
NOTES

1. PIN DESTINATIONS SHOWN AS POSN/PIN e.g. 21/7 INDICATES POSN 21 PIN 7

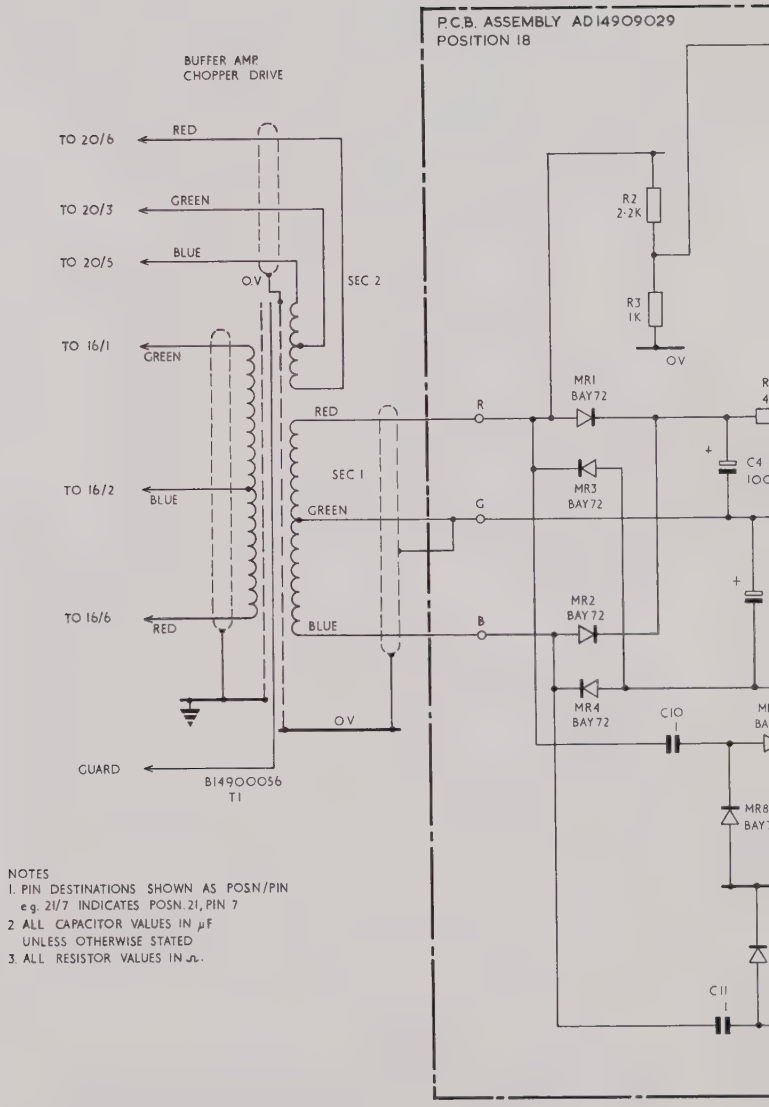

nV OFFSET
RV1 10K
+18V
R30 3·3K
R22 2·2K
R28 1·5M
MR1 SZD5·6
R23 2·2K
R24 2·2K
R29 470K
TO 21/3
OFFSET CONTROL A O T
R25 2·2K
OV
R26 2·2K
MR2 SZD5·6
R27 2·2K
R31 3·3K
-18V
SC 2
RLJ 1
RLK 1
RLK 2
RLJ 2
RLE 1
RLF 1
TO 21/4
TO 21/7
OV
R1 10K
R13 1·2K
C3 0·1
R10 30K
R15 100·25
RV2 20K
SET 20mV
R11 120K
RLB 1
RLC 1
RLC 2
R16 906·3
RV3 20K
SET 200mV
RLB 2
RLG 1
RLD 1
RLD 2
R12 400K
R17 9·202K
RV4 20K
SET 2V
R8 10K
RLE 2
RLA 1
SET 20V
R14 190
REFERENCE ATTENUATOR
RLH 2
RLL 1
RLL 2
RV5 5K
R19 10
R18 89·8K
C4 0·01
R9 300K
RLG 2
RLF 2
TO 20/14
TO 21/1

FLOATING POWER SUPPLY P.C.B. (POSITION NO. 18)

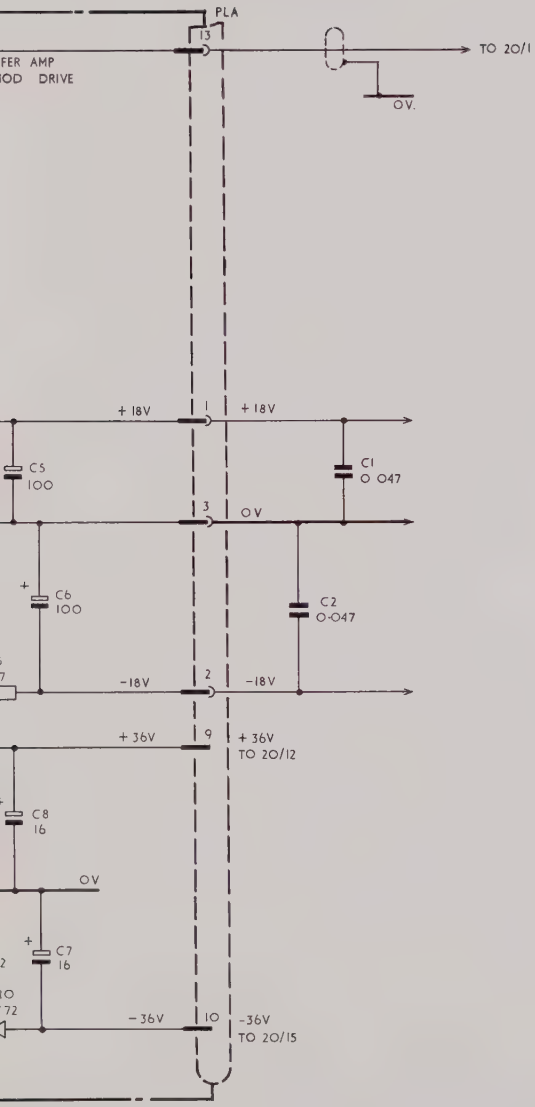
Cct. Ref.		General Description			Solartron Part No.
R2	X	2200	½W	10%	172332200
R3	X	1000	½W	10%	172331000
R4	Y	4.7	2.6W	5%	173404700
R5	Y	4.7	2.6W	5%	173404700
C3 to C6		100	20V	20%	208700037
C7		16	40V	−10% +50%	208600171
C8		16	40V	−10% +50%	208600171
C10		1.0	100V	10%	225461000
C11		1.0	100V	10%	225461000
MR1 to MR4		BAY72			300524530
MR7 to MR10		BAY72			300524530



AD 14909029



NOTES
1. PIN DESTINATIONS SHOWN AS POSN/PIN
   e.g. 21/7 INDICATES POSN. 21, PIN 7
2. ALL CAPACITOR VALUES IN μF
   UNLESS OTHERWISE STATED
3. ALL RESISTOR VALUES IN Ω.


PLA
13
TO 20/1
FER AMP
OD DRIVE
0V.
+18V
1
+18V
C5
100
C1
0·047
3
0V
C6
100
C2
0·047
-18V
2
-18V
+36V
9
+36V
TO 20/12
C8
16
0V
C7
16
-36V
10
-36V
TO 20/15

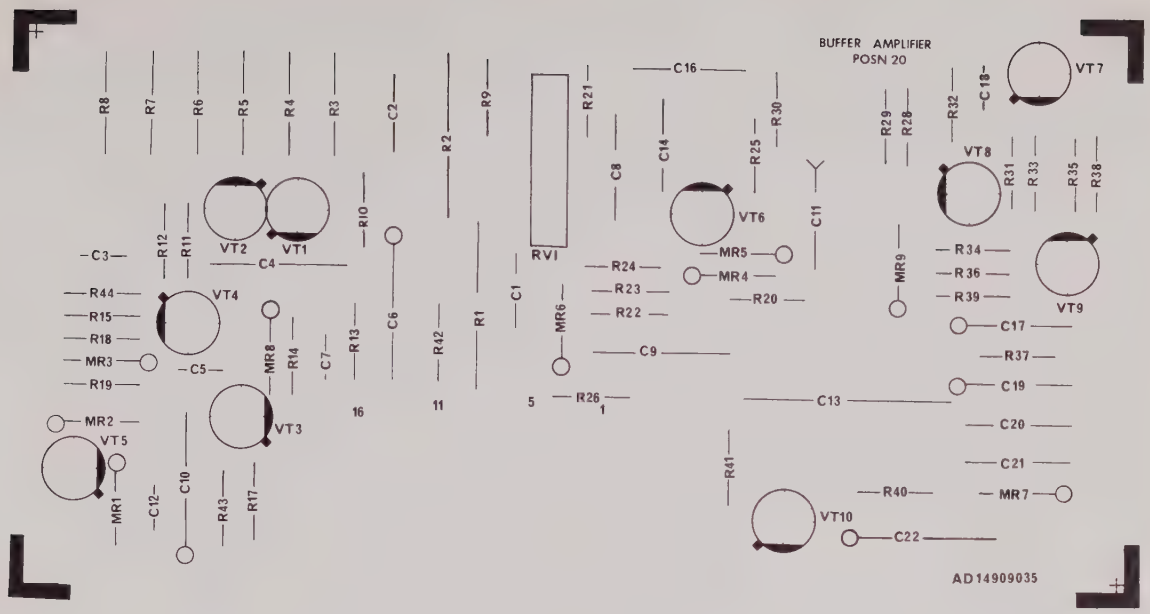
11-11-70 01

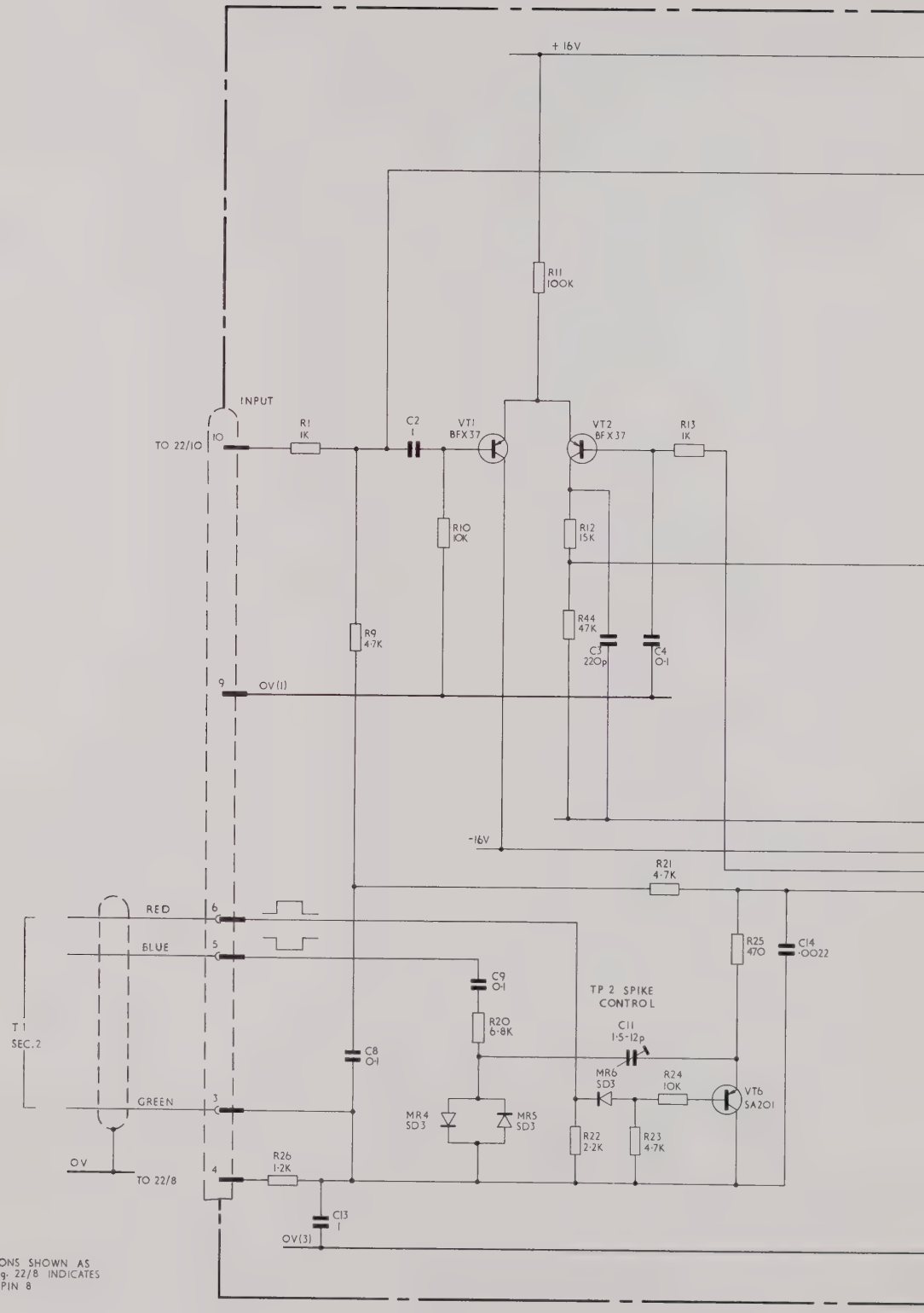
BUFFER AMPLIFIER P.C.B. (POSITION NO. 20)

Cct. Ref.		General Description			Solartron Part No.
R1		1000	¼W	0.1%	B14900046
R2		151.4k	¼W	0.1%	B14900046
R3		10k	1/8W	1%	B14900302
R4		5000	1/8W	1%	B14900302
R5		2500	1/8W	1%	B14900302
R6		1250	1/8W	1%	B14900302
R7	V	620	¼W	1%	198326202
R8	V	330	¼W	1%	198323302
R9	X	4700	½W	10%	172334700
R10	X	10k	½W	10%	172341000
R11	X	100k	½W	10%	172351000
R12	X	15k	½W	10%	172341500
R13	X	1000	¼W	10%	172331000
R14	X	560	½W	10%	172325600
R15	X	3300	½W	10%	172333300
R17	X	10k	½W	10%	172341000
R18	X	330	½W	10%	172323300
R19	X	15k	½W	10%	172341500
R20	X	6800	½W	10%	172336800
R21	X	4700	½W	10%	172334700
R22	X	2200	½W	10%	172332200
R23	X	4700	½W	10%	172334700
R24	X	10k	½W	10%	172341000
R25	X	470	½W	10%	172324700
R26	X	1200	½W	10%	172331200
R28	X	33k	½W	10%	172343300
R29	X	3300	½W	10%	172333300
R30	X	33k	½W	10%	172343300
R31	X	10	½W	10%	172311000
R32	X	3300	½W	10%	172333300
R33	X	270	½W	10%	172322700
R34	X	22k	½W	10%	172342200
R35	X	2200	½W	10%	172332200
R36	X	4700	½W	10%	172334700
R37	X	2200	½W	10%	172332200
R38	X	10	½W	10%	172311000
R39	X	5600	½W	10%	172335600
R40	X	10k	½W	10%	172341000
R41	X	10k	½W	10%	172341000
R42	X	150	½W	10%	172321500
R43	X	330	½W	10%	172323300
R44	X	47k	½W	10%	172344700
RV1		500	1W	5%	122025000

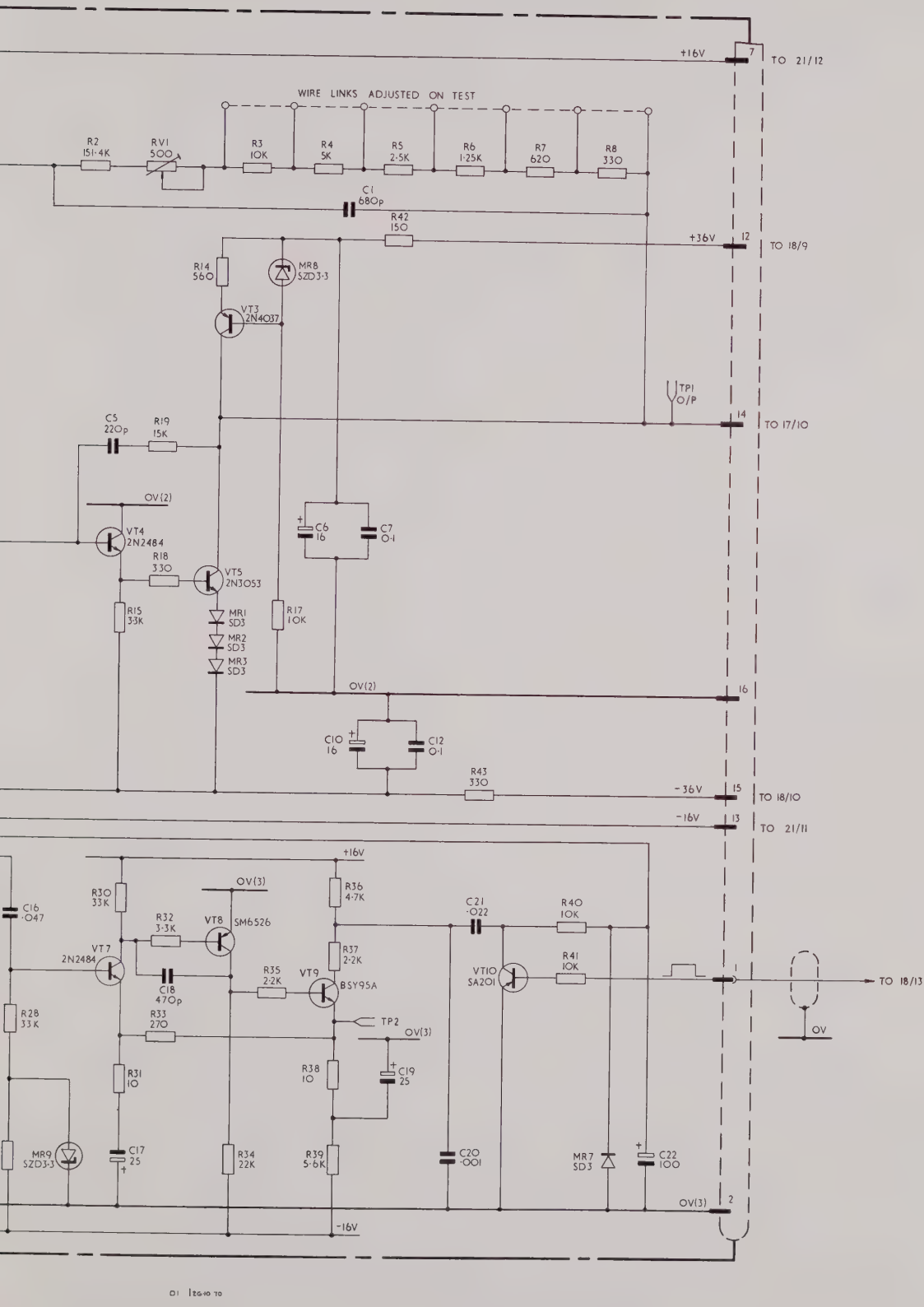
Cct. Ref.	General Description			Solartron Part No.
C1	680p	125V	10%	210226800
C2	1.0	100V	10%	225461000
C3	220p	500V	10%	208400046
C4	0.1	160V	10%	220351000
C5	220p	500V	10%	208400046
C6	16	40V	-10%	
			+50%	208600171
C7	0.1	50V	-20%	
			+80%	208450083
C8	0.1	160V	10%	220351000
C9	0.1	160V	10%	220351000
C10	16	40V	-10%	
			+50%	208600171
C11	12p	1000V		290060030
C12	0.1	50V	-20%	
			+80%	208450083
C13	1.0	160V	10%	220361000
C14	2200p	400V	10%	222332200
C16	.047	160V	10%	220344700
C17	25	12V	-20%	
			+100%	270472500
C18	470p	500V	10%	208400047
C19	25	12V	-20%	
			+100%	270472500
C20	1000p	400V	10%	222331000
C21	.022	160V	10%	220342200
C22	100	10V	10%	265381000

MR1 to MR7	SD3	Solartron	300522160
MR8	SZD3.3	Solartron	300521860
MR9	SZD3.3	Solartron	300521860
VT1	BFX37		300553030
VT2	BFX37		300553030
VT3	2N4037		300553170
VT4	2N2484		300552860
VT5	2N3053		300551800
VT6	SA201		300552640
VT7	2N2484		300552860
VT8	SM526		300552990
VT9	BSY95A		300552280
VT10	SA201		300552640
	Conn. Plug Fxd. 16 Way		352316070


BUFFER AMPLIFIER
POSN 20
R8
R7
R6
R5
R4
R3
C2
R2
R9
R21
C16
C18
VT7
R29
R28
R32
R30
R25
C14
C8
VT8
R31
R33
R35
R38
VT6
C11
VT2
VT1
R10
RV1
C3
R12
R11
C4
R24
MR5
R34
R44
VT4
R23
MR4
R36
R15
R22
R20
MR9
R39
VT9
R18
MR8
R14
C7
R13
C6
R42
R1
C1
MR6
C17
MR3
C5
C9
R37
R19
16
11
5
R26
1
C13
C19
MR2
VT3
C20
VT5
C21
C10
R41
C12
R43
R17
R40
MR7
MR1
VT10
C22
AD14909035



NOTE
1. PIN DESTINATIONS SHOWN AS POSN. / PIN e.g. 22/8 INDICATES POSITION 22, PIN 8


+16V
7
TO 21/12
WIRE LINKS ADJUSTED ON TEST
R2 151·4K
RV1 500
R3 10K
R4 5K
R5 2·5K
R6 1·25K
R7 620
R8 330
C1 680p
R42 150
+36V
12
TO 18/9
R14 560
MR8 SZD3·3
VT3 2N4037
TP1 O/P
C5 220p
R19 15K
14
TO 17/10
OV(2)
VT4 2N2484
C6 16
C7 0·1
R18 330
VT5 2N3053
R15 33K
MR1 SD3
MR2 SD3
MR3 SD3
R17 10K
OV(2)
16
C10 16
C12 0·1
R43 330
-36V
15
TO 18/10
-16V
13
TO 21/11
+16V
OV(3)
R30 33K
R36 4·7K
C16 ·047
R32 3·3K
VT8 SM6526
C21 ·022
R40 10K
VT7 2N2484
R37 2·2K
C18 470p
R35 2·2K
VT9 BSY95A
VT10 SA201
R41 10K
1
TO 18/13
R28 33K
R33 270
TP2
OV(3)
OV
R31 10
R38 10
C19 25
MR9 SZD3·3
C17 25
R34 22K
R39 5·6K
C20 ·001
MR7 SD3
C22 100
OV(3)
2
-16V

INPUT AMPLIFIER P.C.B. (POSITION NO. 21)

Cct. Ref.		General Description			Solartron Part No.
R1	V	10k	1/16W	1%	192641002
R2	X	1M	1/8W	10%	172061000
R3	V	10k	1/16W	1%	192641002
R4	V	220	1/16W	1%	192622202
R5	X	56k	1/8W	10%	172045600
R6	V	2200	1/16W	1%	192632202
R7	X	22k	1/8W	10%	172042200
R8	V	2200	1/16W	1%	192632202
R9	V	180k	1/16W	1%	192651802
R10	V	2200	1/16W	1%	192632202
R11	V	10k	1/16W	1%	192641002
R12	X	1000	1/8W	10%	172031000
R13	X	1M	1/8W	10%	172061000
R14	X	1000	1/8W	10%	172031000
R15	V	15k	1/16W	1%	192641502
R16	V	220	1/16W	1%	192622202
R17	X	56k	1/8W	10%	172045600
R18	V	10k	1/16W	1%	192641002
R19	X	33k	1/8W	10%	172043300
R20	X	6800	1/8W	10%	172036800
R21	X	10k	1/8W	10%	172041000
R22	X	220k	1/8W	10%	172052200
R23	X	33k	1/8W	10%	172043300
R24	X	150	1/8W	10%	172021500
R25	X	1800	1/8W	10%	172031800
R26	X	22k	1/8W	10%	172042200
R27	X	22k	1/8W	10%	172042200
R28	X	3300	1/8W	10%	172033300
R29	X	27k	1/8W	10%	172042700
R30	X	1000	1/8W	10%	172031000
R31	V	68	1/16W	1%	192616802
R32	X	100k	1/8W	10%	172051000
R33	V	560	1/16W	1%	192625602
R34	V	2200	1/16W	1%	192632202
R35	V	10k	1/16W	1%	192641002
R36	X	6800	1/8W	10%	172036800
R37 to R42	X	1000	1/8W	10%	172031000
R43	X	470	1/8W	10%	172024700
R44	X	470	1/8W	10%	172024700
R45	X	100k	1/8W	10%	172051000
R46	V	10	1/16W	1%	192611002
R47	V	100k	1/16W	1%	192651002
R48	X	4700	1/8W	10%	172034700
R49	X	270k	1/8W	10%	172052700
R50	X	3300	1/8W	10%	172033300
R51	X	82	1/8W	10%	172018200
R52	X	39	1/8W	10%	172013900
R53	V	3300	1/16W	1%	192633300
R54	X	33k	1/8W	10%	172043300
R55	V	470	1/16W	1%	192624702
R56	X	1000	1/8W	10%	172031000
RV1		100	½W	10%	110016040
RV2		10K	¼W	5%	130541000

Cct. Ref.	General Description			Solartron Part No.
C1	0.01	100V	10%	225441000
C2	0.047	100V	10%	225444700
C3	82p	350V	5%	250318200
C4	22	15V	20%	265672200
C5	2200p	200V	5%	250332200
C6	3.3	15V	20%	265663300
C7	2200p	200V	5%	250332200
C8	220p	350V	5%	250322200
C9	47	20V	20%	265874700
C10	1000p	500V	20%	241331000
C11	470p	350V	5%	250324700
C12	0.01	100V	10%	225441000
C13	22	15V	20%	265672200
C14	3.3	15V	20%	265663300
C15	15	20V	20%	265871500
C16	0.22	100V	10%	225452200
C17	22	15V	20%	265672200
C18	33p	200V	10%	240713300
C19	33p	200V	10%	240713300
C20 to C23	0.22	100V	10%	225452200
C24	0.047	100V	10%	225444700
C25	0.047	100V	10%	225444700
C26	47	20V	20%	265874700
C27	47	20V	20%	265874700
C28	0.047	25V	+50% −25%	241944700
C29	0.033	100V	10%	225443300

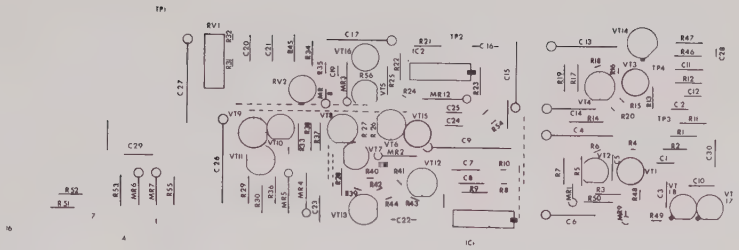
MR1	SZD4.7	300521470
MR2	SD3	300522160
MR3	SD3	300522160
MR4	SZD6.8	300522540
MR5	SZD3.3	300521860
MR6	IN3595	300523590
MR7	IN3595	300523590
MR8	SD3	300522160
MR9	SZD4.7	300521470
MR12	SZD4.7	300521470

VT1	2N4303	300553160
VT2	D1563	300553031
VT3	2N4303	300553160
VT4	D1563	300553031
VT5	D1563	300553031
VT6 to VT13	D2039	300553421
VT14	3N141	300554210
VT15	U1897E	300553800
VT16	U1897E	300553800
VT17	2N2484	300552860
VT18	SA201	300552640

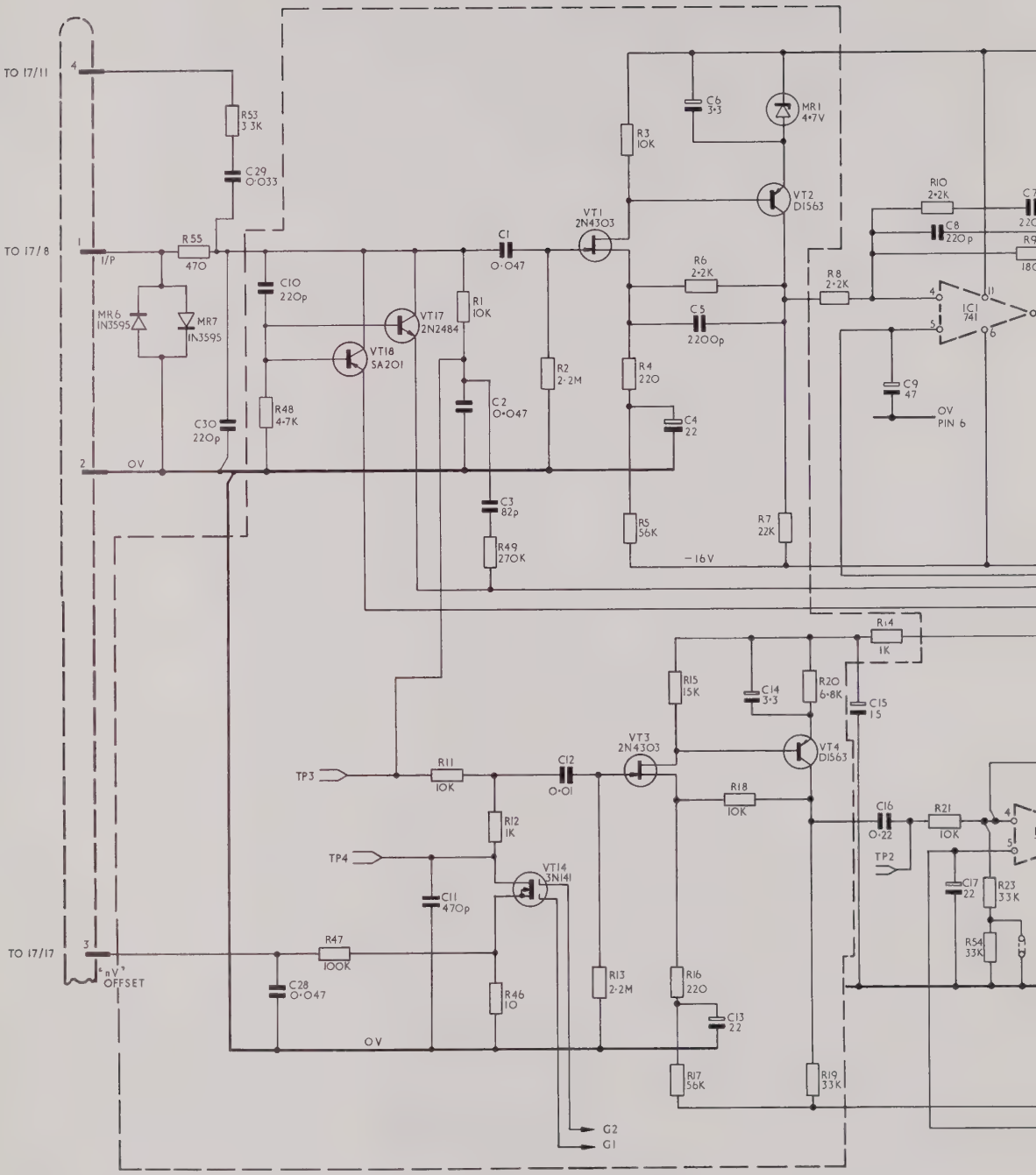
IC1	μA741	510000590
IC2	μA741	510000590

WARNING

ENSURE THAT VT14 (LOCATED IN SCREENED BOX) HAS ITS PINS SHORTED WITH SEVERAL TURNS OF FINE GAUGE WIRE BEFORE ATTEMPTING TO REPAIR OR REPLACE ANY COMPONENT ON THIS BOARD

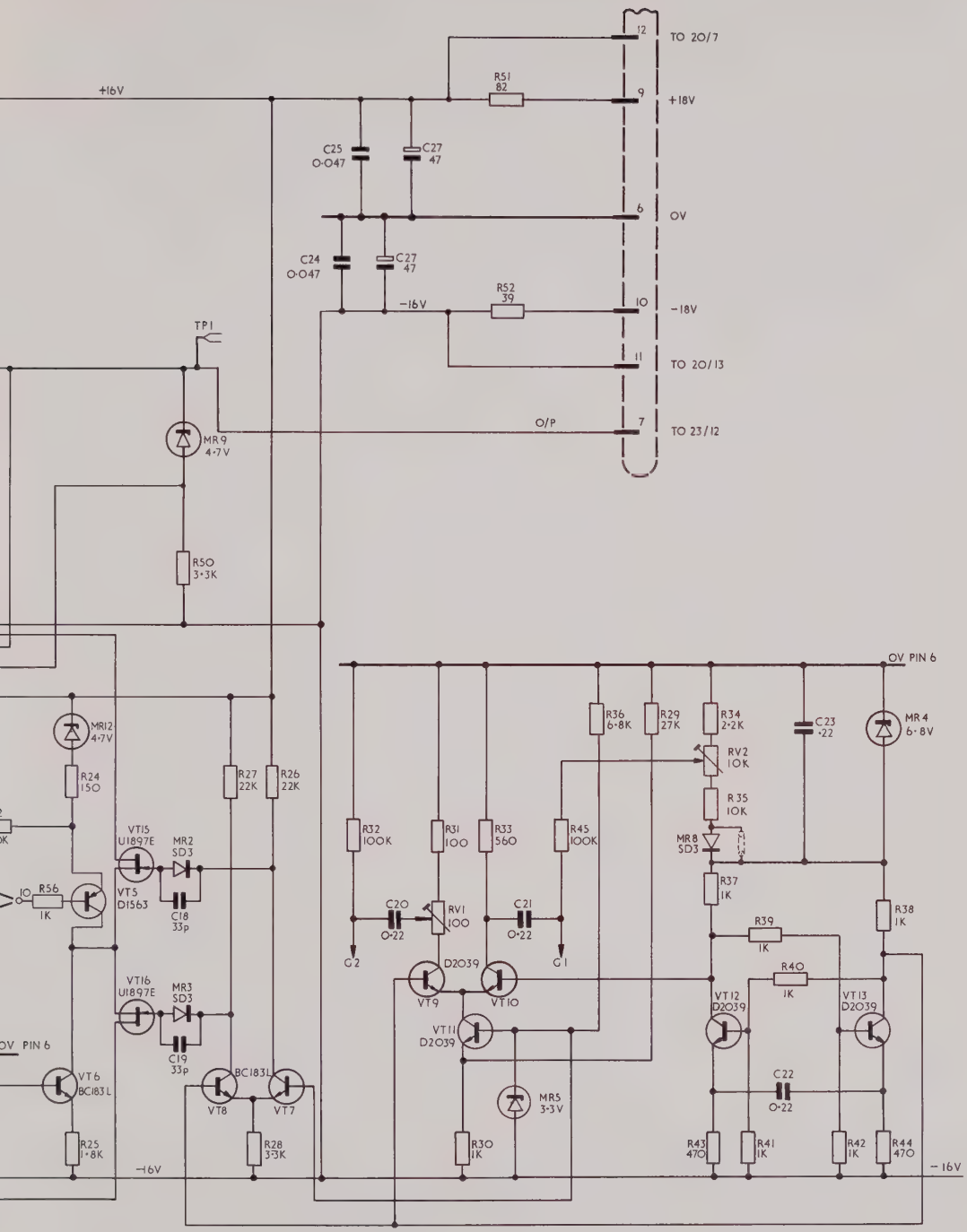


AD14909057



NOTES

1. VT14 IS SUPPLIED WITH A SHORTING CLIP WHICH MUST NOT BE REMOVED UNTIL AMPLIFIER IS READY FOR TEST
2. IF COMPONENTS RV2 R34 R45 R32 HAVE TO BE REPLACED ENSURE THAT VT14 HAS ITS PINS SHORTED WITH SEVERAL TURNS OF FINE GAUGE WIRE BEFORE REMOVING COMPONENT. REMOVE SHORT AFTER NEW COMPONENT IS INSERTED.
3. COMPONENTS ENCLOSED BY THE DOTTED LINE ARE CONTAINED WITHIN THE SCREENED BOX

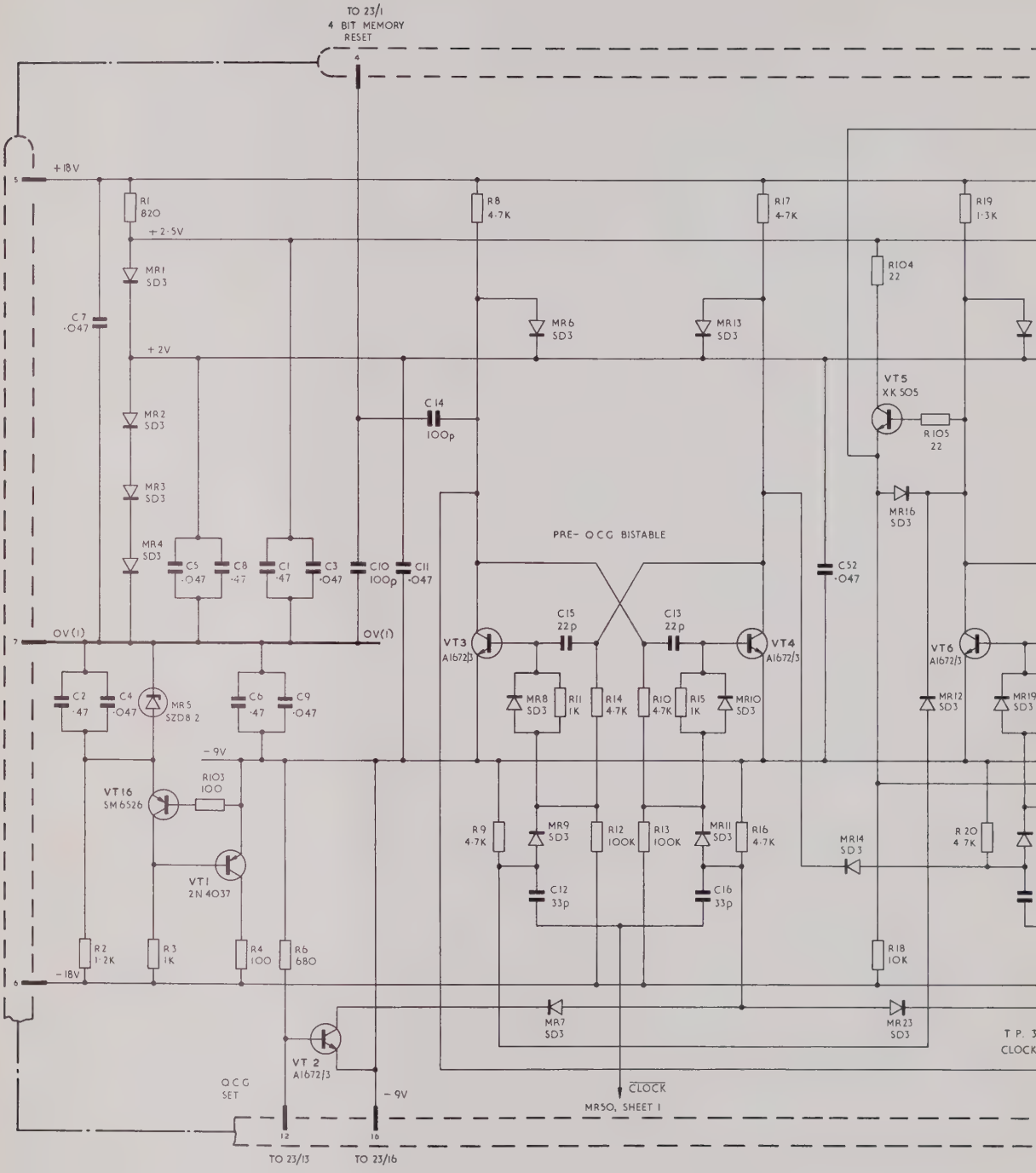

+16V
R51 82
12
TO 20/7
9
+18V
C25 0·047
C27 47
6
0V
C24 0·047
C27 47
−16V
R52 39
10
−18V
TP1
11
TO 20/13
O/P
7
TO 23/12
MR9 4·7V
R50 3·3K
0V PIN 6
MR12 4·7V
R24 150
R27 22K
R26 22K
VT15 U1897E
MR2 SD3
VT5 D1563
C18 33p
R56 1K
VT16 U1897E
MR3 SD3
C19 33p
VT6 BC183L
VT8 BC183L
VT7
R25 1·8K
R28 33K
−16V
R36 6·8K
R29 27K
R34 2·2K
C23 ·22
MR4 6·8V
RV2 10K
R35 10K
R32 100K
R31 100
R33 560
R45 100K
MR8 SD3
R37 1K
R38 1K
C20 0·22
RV1 100
C21 0·22
G2
G1
R39 1K
D2039
VT9
VT10
R40 1K
VT11 D2039
VT12 D2039
VT13 D2039
MR5 3·3V
C22 0·22
R30 1K
R43 470
R41 1K
R42 1K
R44 470
−16V

8.107d

QUANTISED CHARGE GENERATOR P.C.B. (POSITION NO.22)

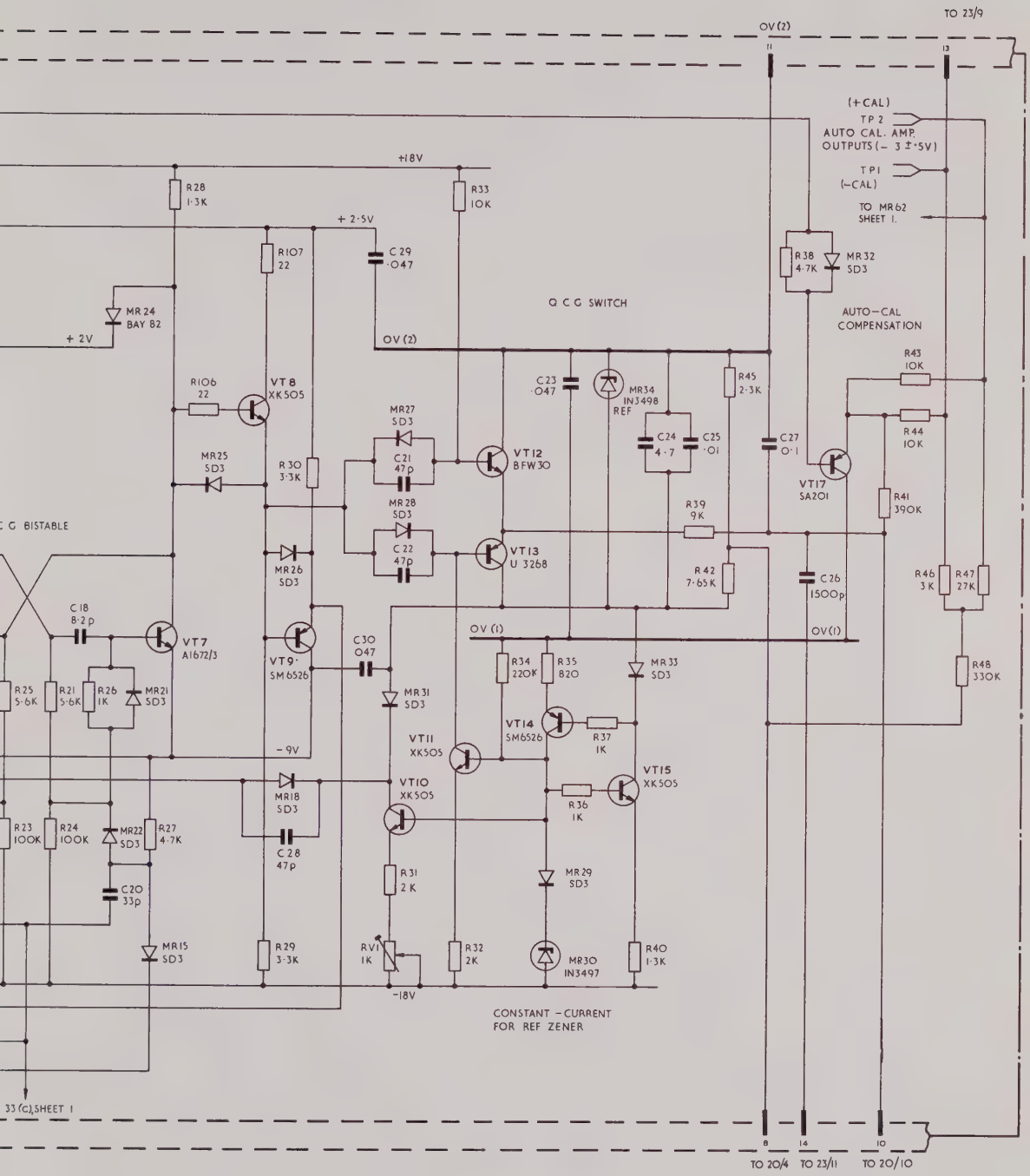
Cct. Ref.		General Description			Solartron Part No.
R1	X	820	½W	10%	172328200
R2	X	1200	½W	10%	172331200
R3	X	1000	½W	10%	172331000
R4	X	100	½W	10%	172321000
R6	X	680	½W	10%	172326800
R8	X	4700	½W	10%	172334700
R9	X	4700	½W	10%	172334700
R10	X	4700	½W	10%	172334700
R11 to R13	X	100k	½W	10%	172351000
R14	X	4700	½W	10%	172334700
R15	X	1000	½W	10%	172331000
R16	X	4700	½W	10%	172334700
R17	X	4700	½W	10%	172334700
R18	X	10k	½W	10%	172341000
R19	Z	1300	½W	10%	195431300
R20	X	4700	½W	10%	172334700
R21	X	5600	½W	10%	172335600
R22 to R24	X	100k	½W	10%	172351000
R25	X	5600	½W	10%	172335600
R26	X	1000	½W	10%	172331000
R27	X	4700	½W	10%	172334700
R28	Z	1300	½W	10%	195431300
R29	X	330	½W	10%	172333300
R30	X	3300	½W	10%	172333300
R31	Z	2000	½W	5%	193532000
R32	Z	2000	½W	5%	193532000
R33	Z	10k	½W	1%	195441000
R34	Z	220k	½W	5%	193552200
R35	Z	820	½W	5%	193528200
R36	X	1000	½W	10%	172331000
R37	X	1000	½W	10%	172331000
R38	X	4700	½W	10%	172334700
R39		9000	As per Spec.		B14900047
R40	Z	1300	½W	5%	193531300
R41	Z	390k	½W	1%	195453900
R42		7650	As per Spec.		B14900047
R43	Z	10k	½W	1%	195441000
R44	Z	10k	½W	1%	195441000
R45		2300	As per Spec.		B14900047
B46	Z	3000	½W	1%	195433300
R47	Z	27k	½W	1%	195442700
R48	Z	330k	½W	1%	195453300
R51	X	2700	½W	10%	172332700
R59	X	3300	½W	10%	172333300
R60	X	220	½W	10%	172322200
R61	X	1200	½W	10%	172331200
R62	X	47K	½W	10%	172344700
R63	X	4700	½W	10%	172334700
R64	X	47k	½W	10%	172324700
R65	X	100	½W	10%	172321000
R66	X	3900	½W	10%	172333900
R67	X	2700	½W	10%	172332700
R68	X	2700	½W	10%	172332700

Cct. Ref.		General Description			Solartron Part No.
R69	X	3900	½W	10%	172333900
R70	X	22k	½W	10%	172342200
R71	X	22k	½W	10%	172342200
R72	X	2700	½W	10%	172332700
R73	X	3900	½W	10%	172333900
R74	X	2700	½W	10%	172332700
R75	X	22k	½W	10%	172342200
R76	X	1000	½W	10%	172331000
R77	X	2700	½W	10%	172332700
R78	Z	4700	½W	1%	195434700
R79	Z	2200	½W	1%	195432200
R80	X	2200	½W	10%	172332200
R81	X	10k	½W	10%	172341000
R82	Z	680	½W	1%	175426800
R83	Z	2200	½W	1%	195432200
R84	Z	4700	½W	1%	195434700
R85	X	10k	½W	10%	172341000
R86	X	10k	½W	10%	172341000
R87	X	10k	½W	10%	172341000
R88	Z	680	½W	1%	195426800
R89	X	1.5M	½W	10%	172361500
R90	X	3.9M	½W	10%	172363900
R91	X	1M	½W	10%	172361000
R92	X	4700	½W	10%	172334700
R95	Z	220k	½W	1%	195452200
R96	X	68	½W	10%	172316800
R97	X	4700	½W	10%	172334700
R99	X	22k	½W	10%	172342200
R101	X	2200	½W	10%	172332200
R102	X	4700	½W	10%	172334700
R103	X	100	¼W	10%	172021000
R104	X	22	¼W	10%	172012200
R105	X	22	¼W	10%	172012200
R106	X	22	¼W	10%	172012200
R107	X	22	¼W	10%	172012200
RV1		1000	1W	5%	122031000
C1		0.47	100V	10%	225454700
C2		0.47	100V	10%	225454700
C3 to C5		0.047	25V	-25% +50%	241944700
C6		0.47	100V	10%	225454700
C7		0.047	25V	-25% +50%	241944700
C8		0.47	100V	10%	225454700
C9		0.047	25V	-25% +50%	241944700
C10		100p	500V	10%	208400044
C11		0.047	25V	-25% +50%	241944700
C12		33p	750V	10%	208400088
C13		22p	750V	10%	240412200
C14		100p	500V	10%	208400044
C15		22p	750V	10%	240412200



NOTES

1 PIN DESTINATIONS SHOWN AS POSN/PIN
e.g. 21/7 INDICATES POSN 21, PIN 7

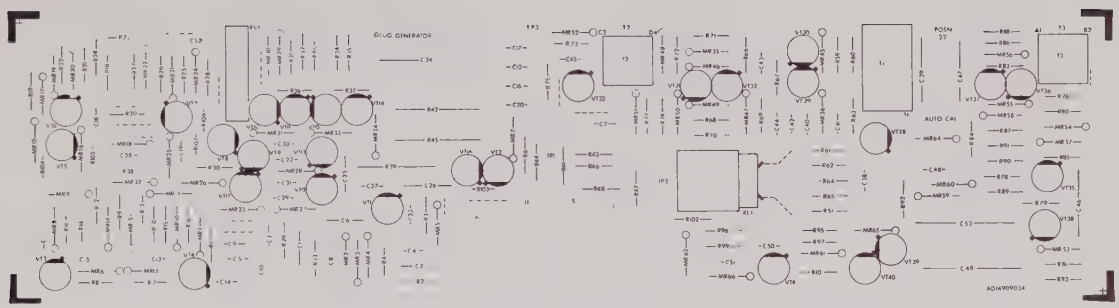

TO 23/9
OV(2)
11
13
(+CAL)
TP 2
AUTO CAL. AMP. OUTPUTS (– 3 ± ·5V)
TP 1
(–CAL)
TO MR62 SHEET 1.
+18V
R28 1·3K
R33 10K
+ 2·5V
R107 22
C29 ·047
R38 4·7K
MR32 SD3
Q C G SWITCH
AUTO–CAL COMPENSATION
MR24 BAY 82
+ 2V
OV(2)
R43 10K
R106 22
VT8 XK505
C23 ·047
MR34 IN3498 REF
R45 2·3K
MR27 SD3
C24 4·7
C25 ·01
C27 0·1
R44 10K
MR25 SD3
R30 3·3K
C21 47p
VT12 BFW30
VT17 SA201
R41 390K
MR28 SD3
R39 9K
C G BISTABLE
C22 47p
VT13 U 3268
MR26 SD3
R42 7·65K
C26 1500p
R46 3K
R47 27K
C18 8·2p
VT7 A1672/3
VT9 SM6526
C30 047
OV(1)
OV(1)
R34 220K
R35 820
MR33 SD3
R48 330K
R25 5·6K
R21 5·6K
R26 1K
MR21 SD3
MR31 SD3
VT14 SM6526
R37 1K
–9V
VT11 XK505
VT15 XK505
MR18 SD3
VT10 XK505
R36 1K
R23 100K
R24 100K
MR22 SD3
R27 4·7K
C28 47p
R31 2K
MR29 SD3
C20 33p
MR15 SD3
R29 3·3K
RV1 1K
R32 2K
MR30 IN3497
R40 1·3K
–18V
CONSTANT – CURRENT FOR REF ZENER
33 (C), SHEET 1
8
14
10
TO 20/4
TO 23/11
TO 20/10

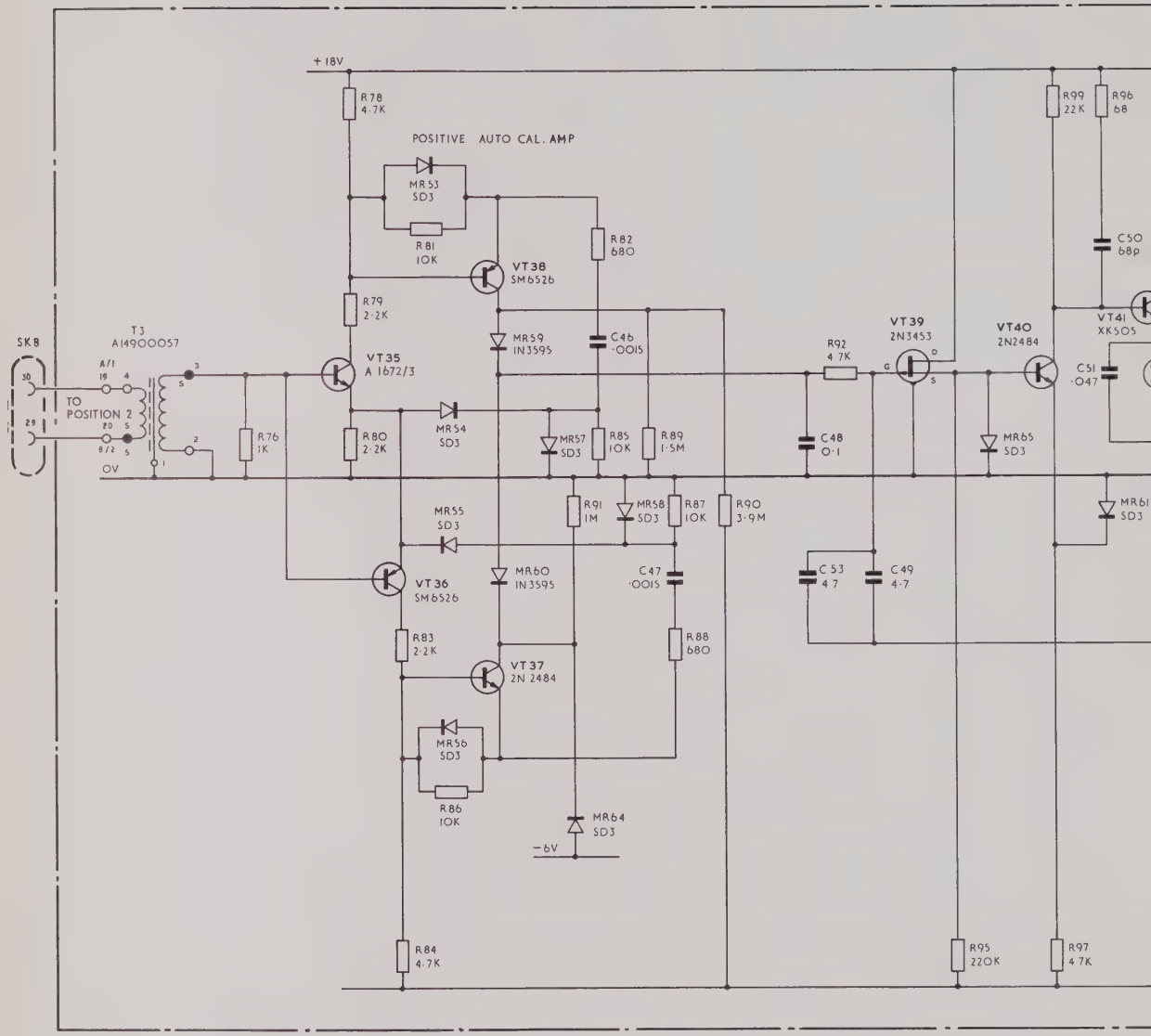
01 | 24·10·70

QUANTISED CHARGE GENERATOR P.C.B. (POSITION NO. 22)

Cct. Ref.	General Description			Solartron Part No.
C16	33p	750V	10%	208400088
C17	33p	750V	10%	208400088
C18	8.2p	750V	10%	208400112
C19	8.2p	750V	10%	208400112
C20	33p	750V	10%	208400088
C21	47p	750V	10%	240414700
C22	47p	750V	10%	240414700
C23	0.047	25V	-25% +50%	241944700
C24	4.7	100V	10%	219864700
C25	.01	500V	25%	208400109
C26	1500p	125V	1%	210031500
C27	0.1	100V	10%	225451000
C28	47p	750V	10%	240414700
C29	0.047	25V	-25% +50%	241944700
C30	0.047	25V	-25% +50%	241944700
C38	.01	400V	10%	226041000
C39	3300p	125V	10%	210233301
C40	0.047	25V	-25% +50%	241944700
C41	47p	750V	10%	240414700
C42	0.047	25V	-25% +50%	241944700
C43 to C45	47p	750V	10%	240414700
C46	1500p	125V	1%	210031500
C47	1500p	125V	1%	210031500
C48	0.1	100V	20%	225551000
C49	4.7	100V	10%	219864700
C50	68p	500V	10%	208400098
C51	0.047	25V	-25% +50%	241944700
C52	0.047	25V	-25% +50%	241944700
C53	4.7	100V	10%	219864700
MR1 to MR4	SD3	Solartron		300522160
MR5	SZD 8.2	Solartron		300521330
MR6 to MR16	SD3	Solartron		300522160
MR17	BAY 82			300524600
MR18 to MR23	SD3	Solartron		300522160
MR24	BAY 82			300524600
MR25 to MR29	SD3	Solartron		300522160
MR30	IN3497			300522800

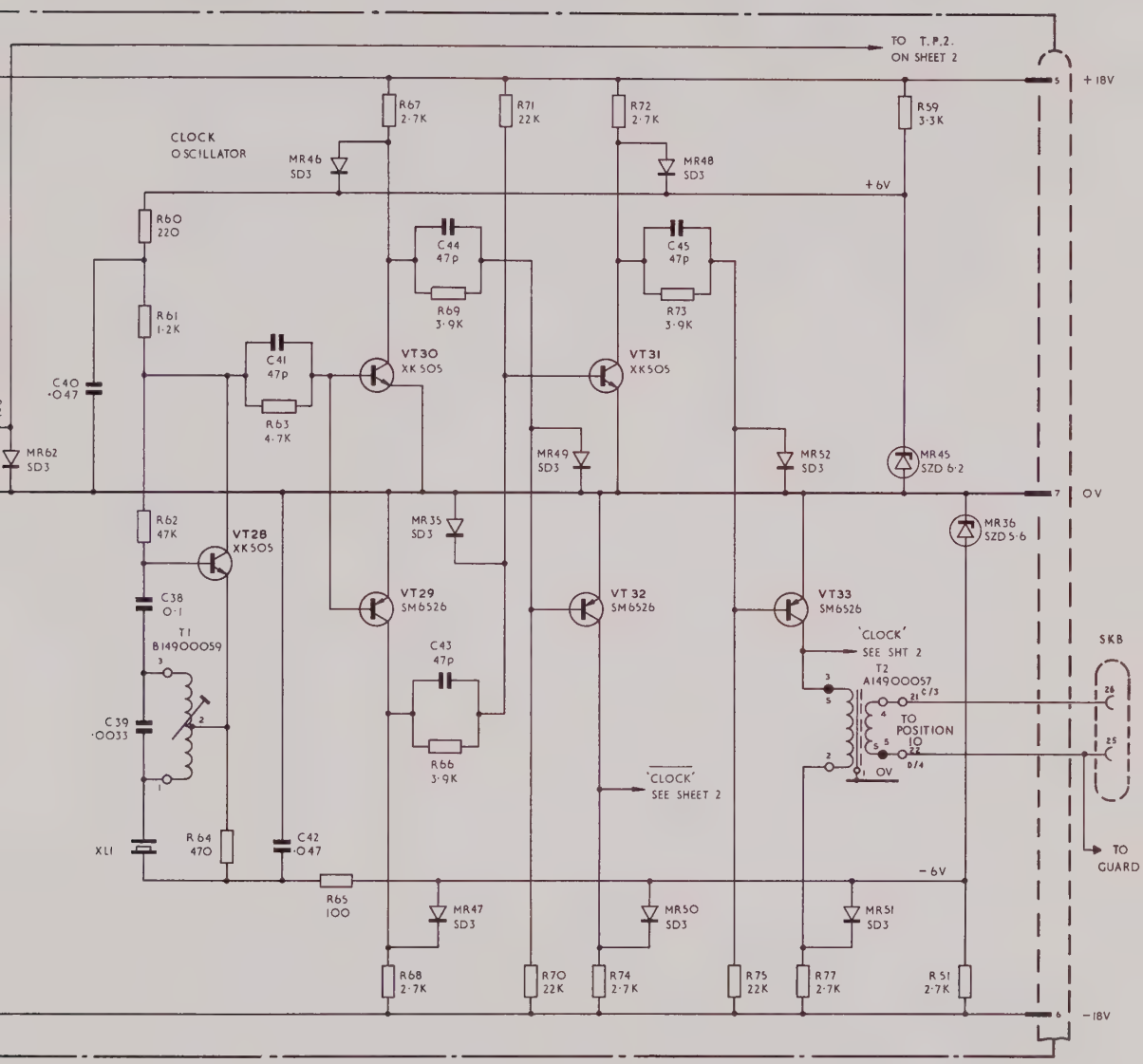
Cct. Ref.	General Description		Solartron Part No.
MR31	SD3	Solartron	300522160
MR32	SD3	Solartron	300522160
MR33	SD3	Solartron	300522160
MR34	IN3498		300524210
MR35	SD3	Solartron	300522160
MR36	SZD 5.6	Solartron	300521450
MR45	SZD6.2	Solartron	300521240
MR46 to MR58	SD3	Solartron	300522160
MR59	IN3595		300523590
MR60	IN3595		300523590
MR61	SD3	Solartron	300522160
MR62	SD3	Solartron	300522160
MR64	SD3	Solartron	300522160
MR65	SD3	Solartron	300522160
MR66	SZD6.2	Solartron	300521240
VT1	2N4037		300553170
VT2 to VT4	A1672/3		300551910
VT5	XK505		300551650
VT6	A1672/3		300551910
VT7	A1672/3		300551910
VT8	XK505		300551650
VT9	SM6526		300552990
VT10	XK505		300551650
VT11	XK505		300551650
VT12	BFW30		300554070
VT13	U3268		300552130
VT14	SM6526		300552990
VT15	XK505		300551650
VT16	SM6526		300552990
VT17	SA201		300552640
VT29	SM6526		300552990
VT30	XK505		300551650
VT31	XK505		300551650
VT32	SM6526		300552990
VT33	SM6526		300552990
VT35	A1672/3		300551910
VT36	SM6526		300552990
VT37	2N2484		300552860
VT38	SM6526		300552990
VT39	2N3453		300553230
VT40	2N2480		300552860
VT41	XK505		300551650
XL1	320KH for 50H OP		A14900101
T1	Transformer (Oscillator)		B14900059
T2	Transformer (Pulse)		B14900057
T3	Transformer (Pulse)		B14900057
	Conn. Plug 16 Way		352316070


GLUG GENERATOR
POSN
AUTO CAL
AD1409034



NOTE

1. XL1 320 kHz FOR 50Hz MAINS (A14900101)
2. XL1 384 kHz FOR 60Hz MAINS (A14900102)
3. PIN DESTINATIONS SHOWN AS POS^{N}/ PIN
   e.g. 21/7 INDICATES POS^{N} 21 PIN 7

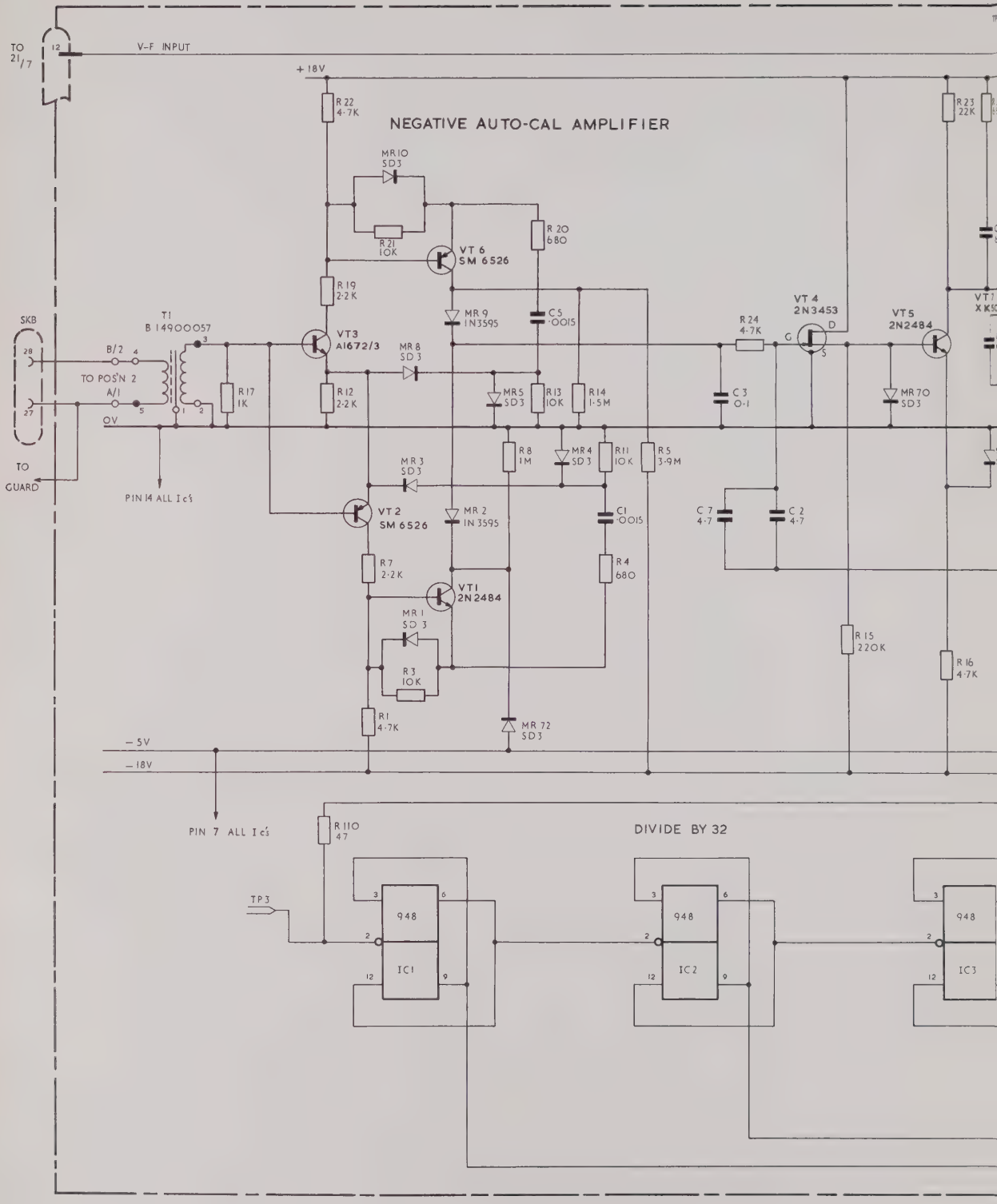

TO T.P.2. ON SHEET 2
+18V
CLOCK OSCILLATOR
R67 2·7K
R71 22K
R72 2·7K
R59 3·3K
MR46 SD3
MR48 SD3
+6V
R60 220
R61 1·2K
C44 47p
R69 3·9K
C45 47p
R73 3·9K
C40 ·047
C41 47p
R63 4·7K
VT30 XK505
VT31 XK505
MR62 SD3
MR49 SD3
MR52 SD3
MR45 SZD 6·2
0V
R62 47K
VT28 XK505
MR35 SD3
MR36 SZD 5·6
C38 0·1
T1 B14900059
VT29 SM6526
VT 32 SM6526
VT33 SM6526
'CLOCK' SEE SHT 2
SKB
C43 47p
T2 A14900057
C39 ·0033
R66 3·9K
TO POSITION 10
'CLOCK' SEE SHEET 2
XL1
R64 470
C42 ·047
R65 100
-6V
MR47 SD3
MR50 SD3
MR51 SD3
TO GUARD
R68 2·7K
R70 22K
R74 2·7K
R75 22K
R77 2·7K
R51 2·7K
-18V

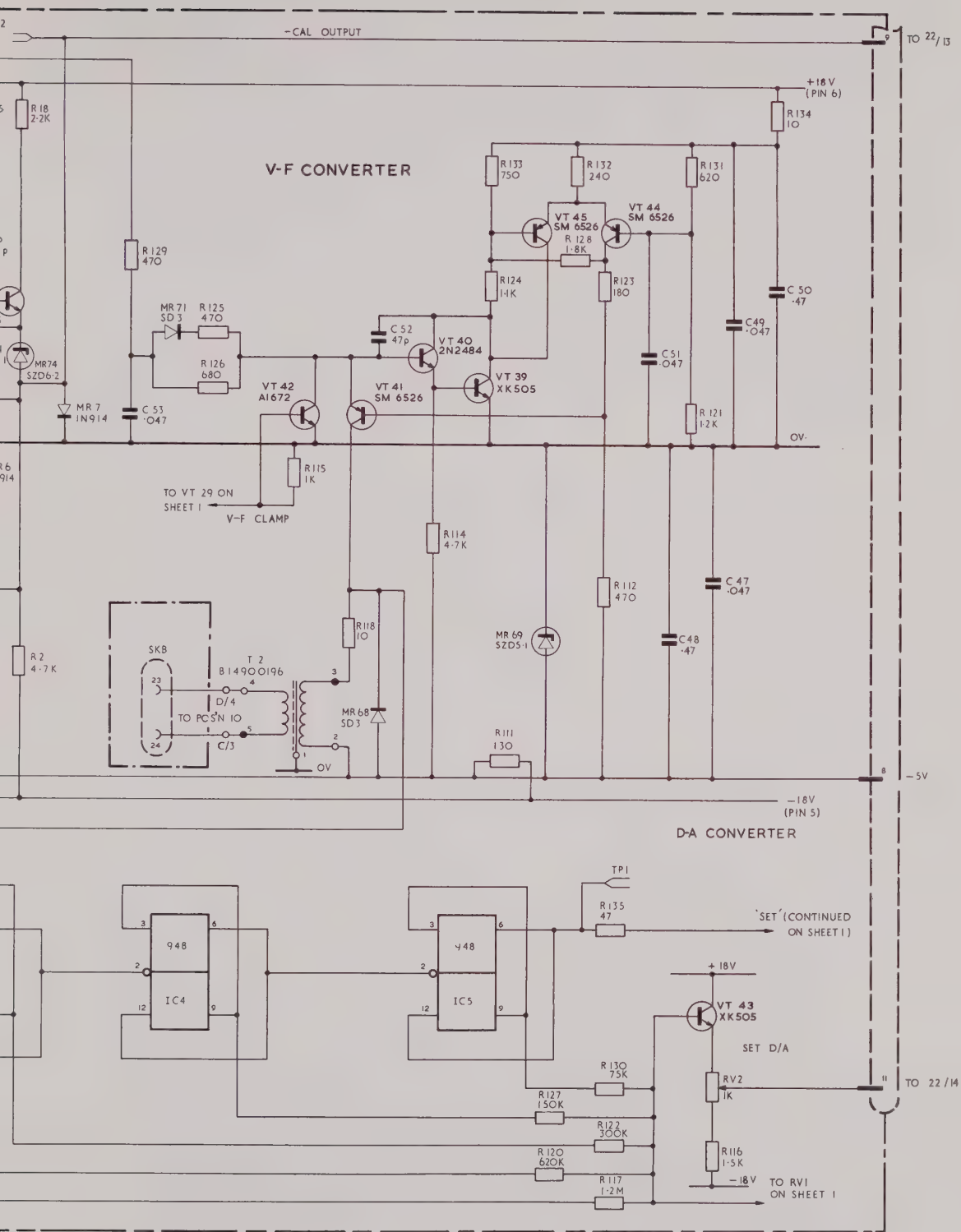
01	26 10 70

V-f CONVERTER AND NEGATIVE AUTO-CAL AMPLIFIER POSITION 23

Cct. Ref.		General Description			Solartron Part No.
R1	X	4700	½W	1%	195434700
R2	X	4700	½W	10%	172334700
R3	X	10K	½W	10%	172341000
R4	X	680	½W	1%	195426800
R5	X	3.9M	½W	10%	172363900
R7	X	2200	½W	1%	195432200
R8	X	1M	½W	10%	172361000
R11	X	10k	½W	10%	172341000
R12	X	2200	½W	10%	172332200
R13	X	10k	½W	10%	172341000
R14	X	1.5M	½W	10%	172361500
R15	Z	220k	½W	1%	195452200
R16	X	4700	½W	10%	172334700
R17	X	1000	½W	10%	172331000
R18	X	2200	½W	10%	172332200
R19	X	2200	½W	1%	195432200
R20	Z	680	½W	1%	195426800
R21	X	10k	½W	10%	172341000
R22	X	4700	½W	1%	195434700
R23	X	22k	½W	10%	172342200
R24	X	4700	½W	10%	172334700
R25	X	68	½W	10%	172316800
R62 to R64	X	270K	½W	10%	172352700
R65 to R72	X	22k	½W	10%	172342200
R73 to R89	X	33k	½W	10%	172343300
R90	X	15k	½W	10%	172341500
R91	X	180k	½W	10%	172351800
R92	X	180k	½W	10%	172351800
R93	X	33k	½W	10%	172343300
R94	X	33k	½W	10%	172343300
R95 to R100	X	180k	½W	10%	172351800
R101	X	4700	½W	10%	172334700
R102	X	8200	½W	10%	172338200
R103	Z	4700	½W	1%	195434700
R104	Z	4700	½W	1%	195434700
R110	X	47	½W	10%	172314700
R111	Z	130	2W	5%	193021300
R112	X	470	½W	10%	172324700
R114	X	4700	½W	10%	172334700
R115	X	1000	½W	10%	172331000
R116	X	1500	½W	10%	172331500
R117	X	1.2M	½W	10%	172361200
R118	X	10	½W	10%	172311000

Cct. Ref.		General Description			Solartron Part No.
R120	Z	620k	½W	5%	193556200
R121	Z	1200	½W	1%	195431200
R122	Z	300k	½W	1%	195453000
R123	X	180	½W	10%	172321800
R124	Z	1100	½W	1%	195431100
R125	Z	470	½W	5%	193524700
R126	Z	680	½W	5%	193526800
R127	Z	150k	½W	1%	195451500
R128	Z	1800	½W	1%	195431800
R129	Z	470	½W	5%	193524700
R130	Z	75k	½W	1%	195447500
R131	Z	620	½W	1%	195426200
R132	Z	240	½W	1%	195422400
R133	Z	750	½W	1%	195427500
R134	X	10	½W	10%	172311000
R135	X	47	½W	10%	172314700
RV1		5000	½W	10%	121255000
RV2		1000	½W	10%	121231000
C1		1500p	125V	1%	210031500
C2		4.7	100V	10%	219864700
C3		0.1	100V	10%	225451000
C4		0.1	100V	10%	225451000
C5		1500p	125V	1%	210031500
C6		68p	750V	10%	240416800
C7		4.7	100V	10%	219864700
C16		0.047	25V	-25% +50%	241944700
C17		0.047	25V	-25% +50%	241944700
C18 to C25		15p	750V	10%	208400041
C26		33p	750V	10%	208400088
C27		0.047	25V	-25% +50%	241944700
C28		33p	750V	10%	208400088
C29		47p	750V	5%	208400008
C30		33p	750V	10%	208400088
C33p					
C31		33p	750V	10%	208400088
C32		47p	750V	5%	208400008
C33 to C36		33p	750V	10%	208400088
C47		0.047	25V	-25% +50%	241944700
C48		0.47	100V	10%	225454700
C49		0.047	25V	-25% +50%	241944700
C50		0.47	100V	10%	225454700
C51		0.047	25V	-25% +50%	241944700
C52		47p	750V	5%	208400008
C53		0.047	25V	-25% +50%	241944700


NEGATIVE AUTO-CAL AMPLIFIER
TO 21/7
12
V-F INPUT
+18V
R22 4·7K
R23 22K
MR10 SD3
R21 10K
VT6 SM6526
R20 680
R19 2·2K
MR9 IN3595
C5 ·0015
VT4 2N3453
VT5 2N2484
R24 4·7K
SKB
28
27
T1 B14900057
B/2
A/1
TO POS'N 2
VT3 AI672/3
MR8 SD3
R17 1K
R12 2·2K
MR5 SD3
R13 10K
R14 1·5M
C3 0·1
MR70 SD3
0V
TO GUARD
PIN 14 ALL I cs
R8 1M
MR4 SD3
R11 10K
R5 3·9M
MR3 SD3
VT2 SM6526
MR2 IN3595
C1 ·0015
C7 4·7
C2 4·7
R7 2·2K
R4 680
VT1 2N2484
MR1 SD3
R3 10K
R15 220K
R16 4·7K
R1 4·7K
MR72 SD3
−5V
−18V
PIN 7 ALL I cs
R110 47
DIVIDE BY 32
TP3
948
IC1
IC2
IC3



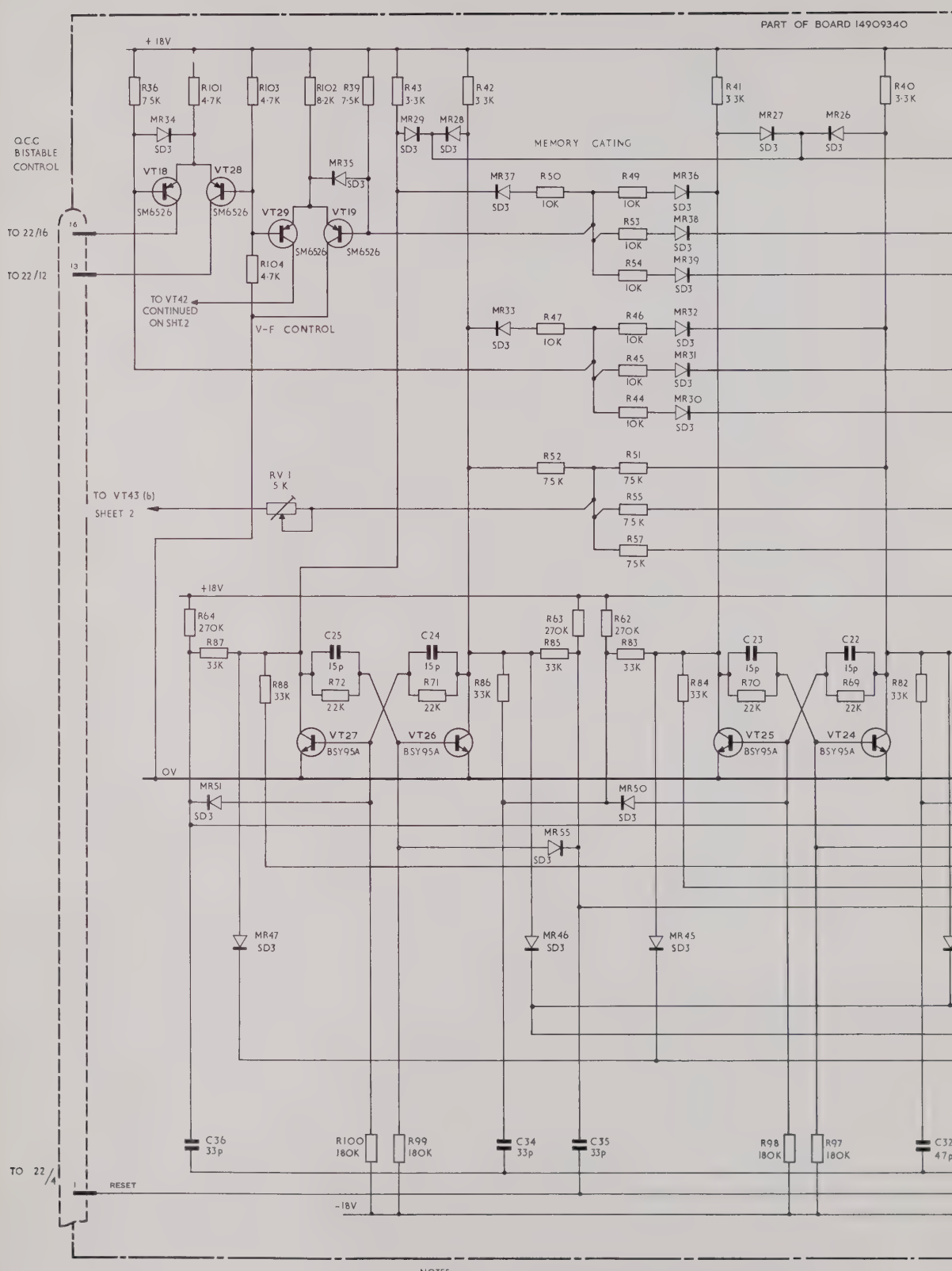
01 28·10·70

D14909340/1

V-f CONVERTER AND NEGATIVE AUTO-CAL AMPLIFIER POSITION 23

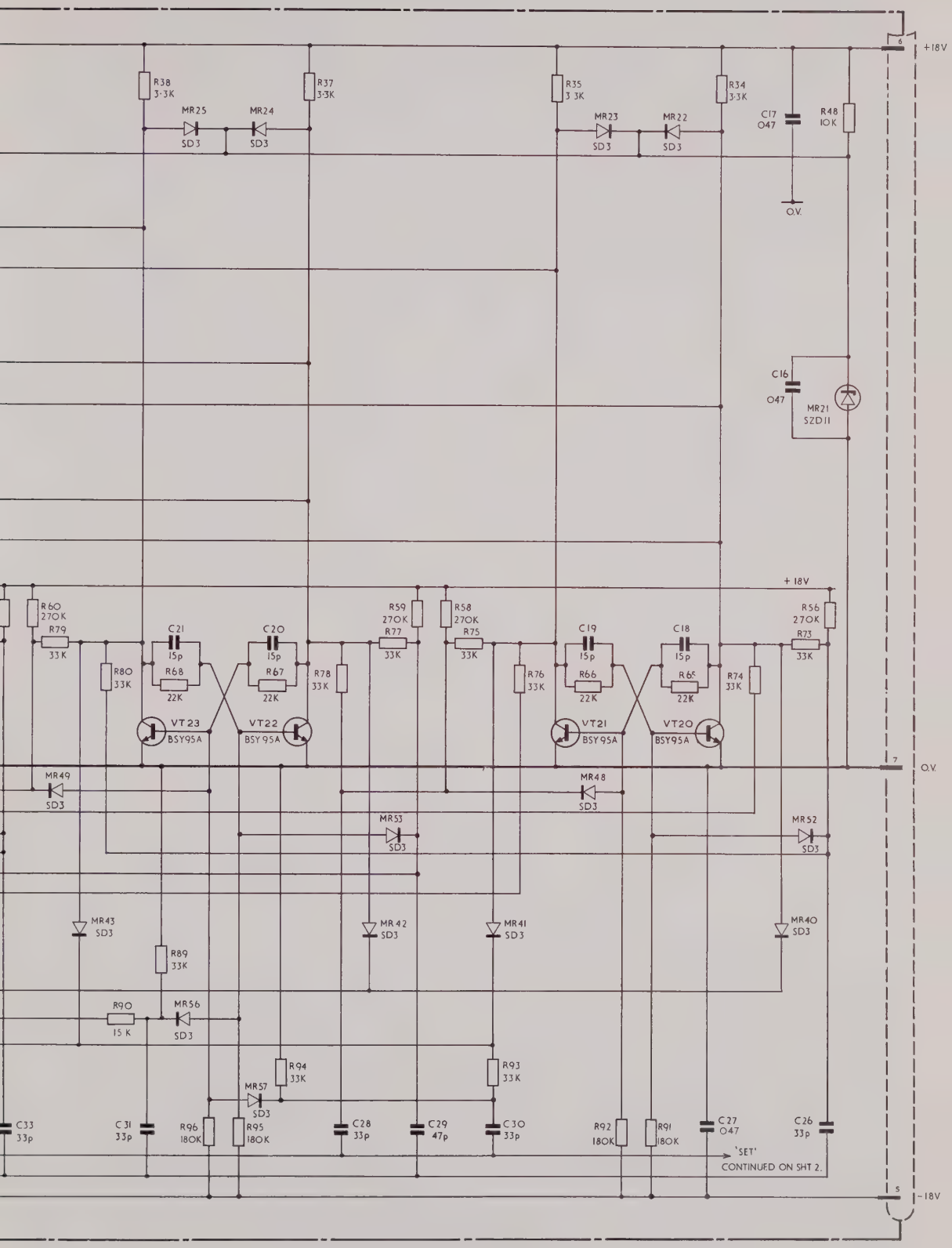
V-f CONVERTER AND NEGATIVE AUTO-CAL AMPLIFIER POSITION 23 (Cont.)

Cct. Ref.	General Description		Solartron Part No.
MR1	SD3	Solartron	300522160
MR2	IN3595		300523590
MR3	SD3	Solartron	300522160
MR4 to MR8	SD3	Solartron	300522160
MR9	IN3595		300523590
MR10	SD3	Solartron	300522160
MR21	SZD11	Solartron	300523910
MR22 to MR57	SD3	Solartron	300522160
MR68	SD3	Solartron	300522160
MR69	SZD5.1	Solartron	300521310
MR70	SD3	Solartron	300522160
MR71	SD3	Solartron	300522160
MR72	SD3	Solartron	300522160
MR74	SZD6.2	Solartron	300521240
VT1	2N2484		300552860
VT2	SM6526		300552990
VT3	A1672/3		300551910
VT4	2N3453		300553230
VT5	2N2484		300552860
VT6	SM6526		300552990
VT7	XK505		300551650
VT18	SM6526		300552990
VT19	SM6526		300552990
VT20 to VT27	BSY95A		300552280
VT28	SM6526		300552990
VT29	SM6526		300552990
VT39	XK505		300551650
VT40	2N2484		300552860
VT41	SM6526		300552990
VT42	A1472/3		300551910
VT43	XK505		300551650
VT44	SM6526		300552990
VT45	SM6526		300552990
IC1 to IC5	I.C. 948 Clock Flip-Flop		510000170
T1	Transformer		B14900057
T2	Transformer		B14900196



NOTES

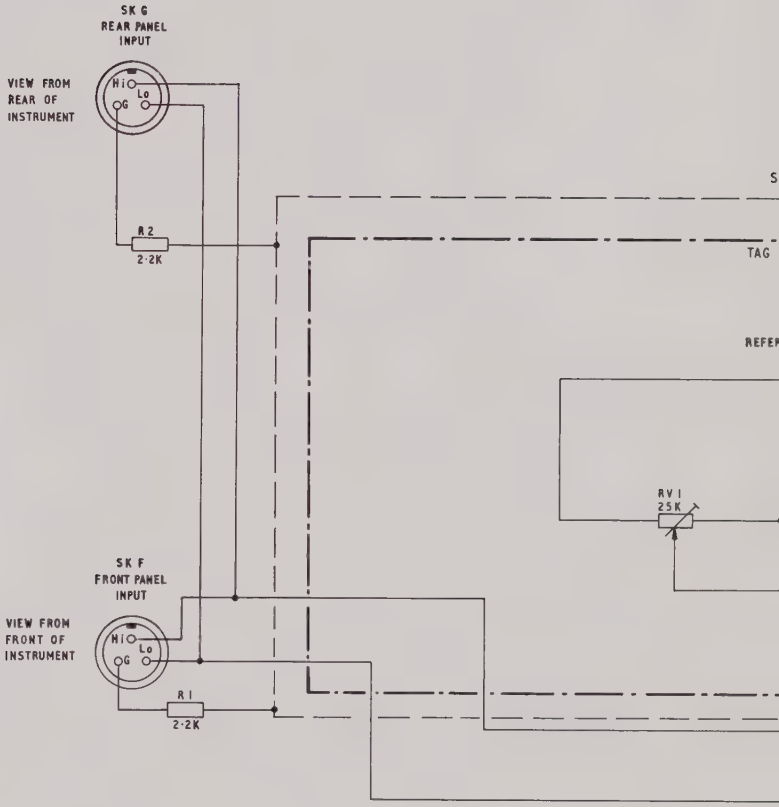
1. PIN DESTINATIONS SHOWN AS POSN/PIN e.g. 22/12 INDICATES POSN 22, PIN 12

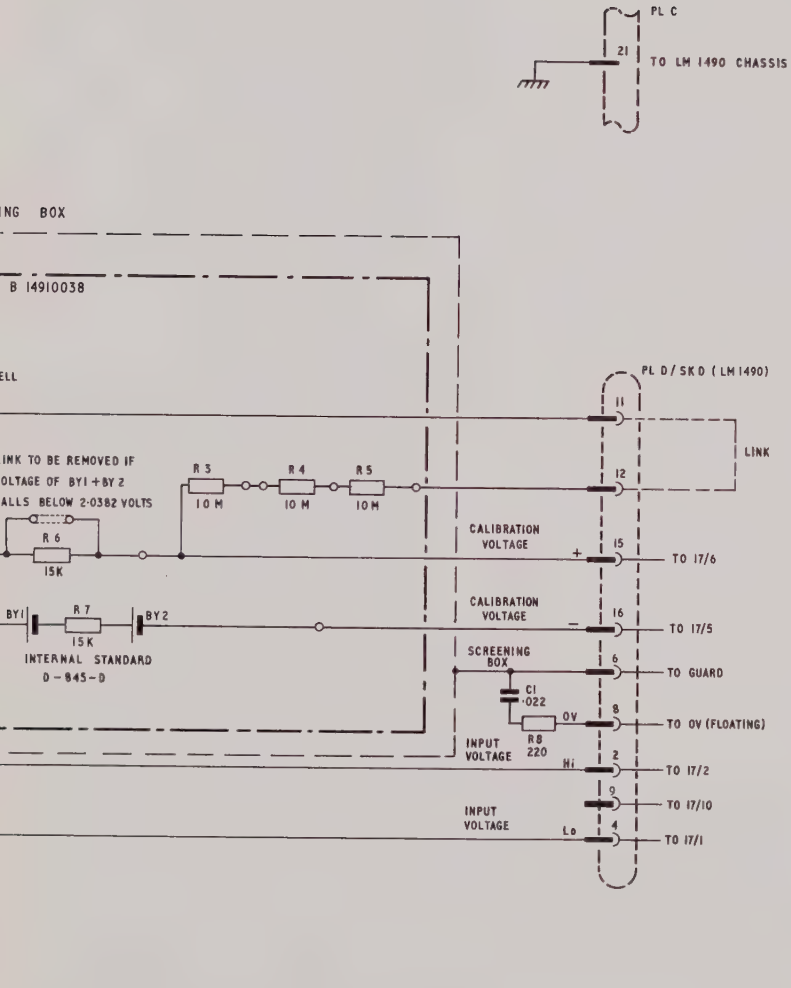

+18V
R38 3·3K
R37 3·3K
MR25 SD3
MR24 SD3
R35 3·3K
R34 3·3K
MR23 SD3
MR22 SD3
C17 047
R48 10K
O.V.
C16 047
MR21 SZD11
+18V
R60 270K
R79 33K
R80 33K
C21 15p
R68 22K
C20 15p
R67 22K
R78 33K
R59 270K
R77 33K
R58 270K
R75 33K
R76 33K
C19 15p
R66 22K
C18 15p
R65 22K
R74 33K
R56 270K
R73 33K
VT23 BSY95A
VT22 BSY95A
VT21 BSY95A
VT20 BSY95A
O.V.
MR49 SD3
MR48 SD3
MR53 SD3
MR52 SD3
MR43 SD3
MR42 SD3
MR41 SD3
MR40 SD3
R89 33K
R90 15 K
MR56 SD3
R94 33K
R93 33K
MR57 SD3
C33 33p
C31 33p
R96 180K
R95 180K
C28 33p
C29 47p
C30 33p
R92 180K
R91 180K
C27 0·47
C26 33p
'SET'
CONTINUED ON SHT 2.
-18V

DC UNIT EX1491

Cct. Ref.		General Description			Solartron Part No.
R1	X	10	1/8W	10%	172011000
R2	X	10	1/8W	10%	172011000
R3 to R5	V	10M	1W	1%	198971002
R6	V	15k	¼W	1%	198341502
R7	V	15k	¼W	1%	198341502
R8	X	220	1/8W	10%	172022200
RV1		25k	1W	5%	121942500

Cct. Ref.		General Description			Solartron Part No.
C1	B	.022	160V	± 10%	220342200
PLC		Conn. Plug 24 Way			352324120
PLD		Plug Fixed 16 Way			352316080
SKF		Conn. Hermpt. Fixed			352803010
SKG		Conn. Hermpt. Fixed			352803010
BY1 to BY3		Ref. Cell Muirhead D-845-D			310010010


SK G
REAR PANEL
INPUT
VIEW FROM
REAR OF
INSTRUMENT
Hi
Lo
G
R2
2·2K
TAG
RV1
25K
SK F
FRONT PANEL
INPUT
VIEW FROM
FRONT OF
INSTRUMENT
Hi
Lo
G
R1
2·2K


PL C
21
TO LM 1490 CHASSIS
NG BOX
B 14910038
ELL
PL D/SK D (LM 1490)
11
LINK
INK TO BE REMOVED IF
OLTAGE OF BY1 + BY 2
ALLS BELOW 2·0382 VOLTS
R 3
10 M
R 4
10 M
R 5
10 M
12
R 6
15K
CALIBRATION VOLTAGE
+
15
TO 17/6
BY1
R 7
15K
BY2
INTERNAL STANDARD
D-845-D
CALIBRATION VOLTAGE
−
16
TO 17/5
SCREENING BOX
6
TO GUARD
C1
·022
0V
8
TO 0V (FLOATING)
INPUT VOLTAGE
R8
220
Hi
2
TO 17/2
9
TO 17/10
INPUT VOLTAGE
Lo
4
TO 17/1

264070 02

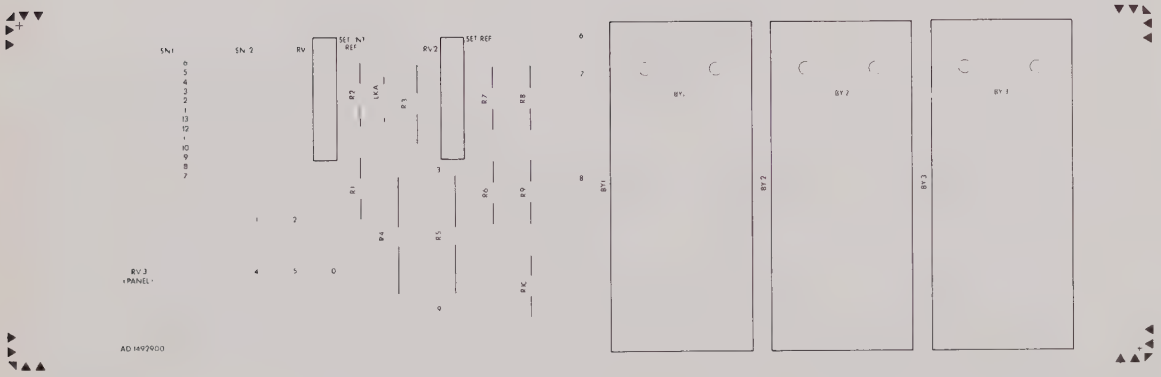
EXTERNAL CALIBRATION UNIT EX1492

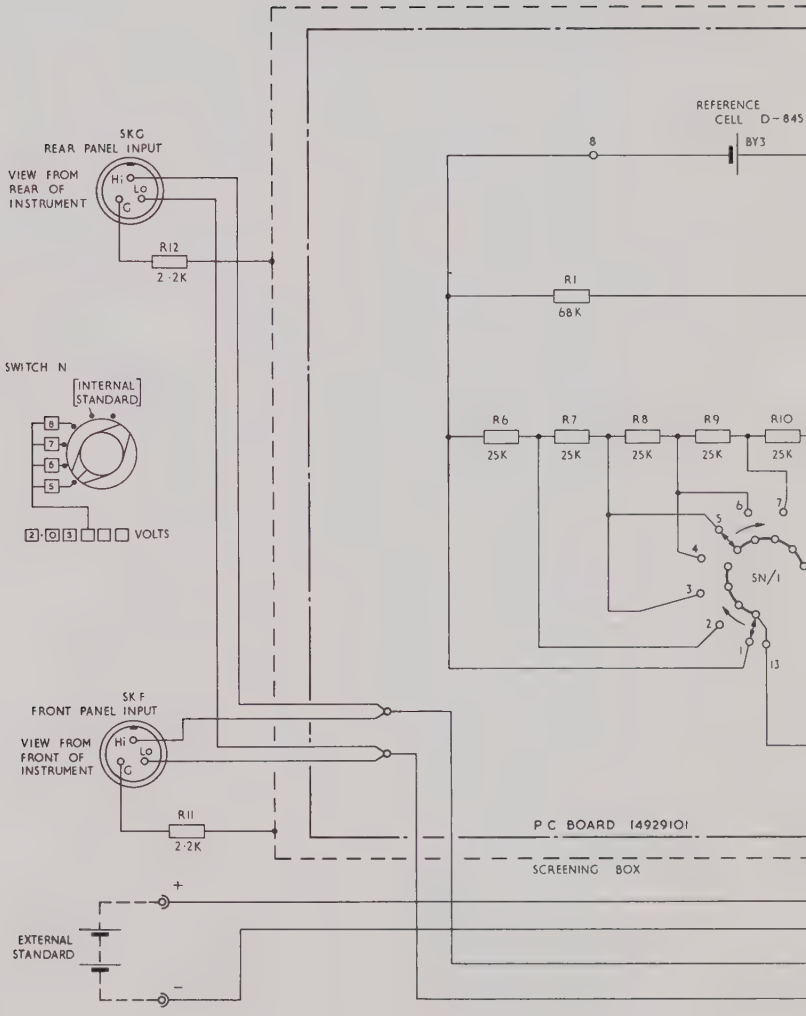
P.C.B. ASSY.

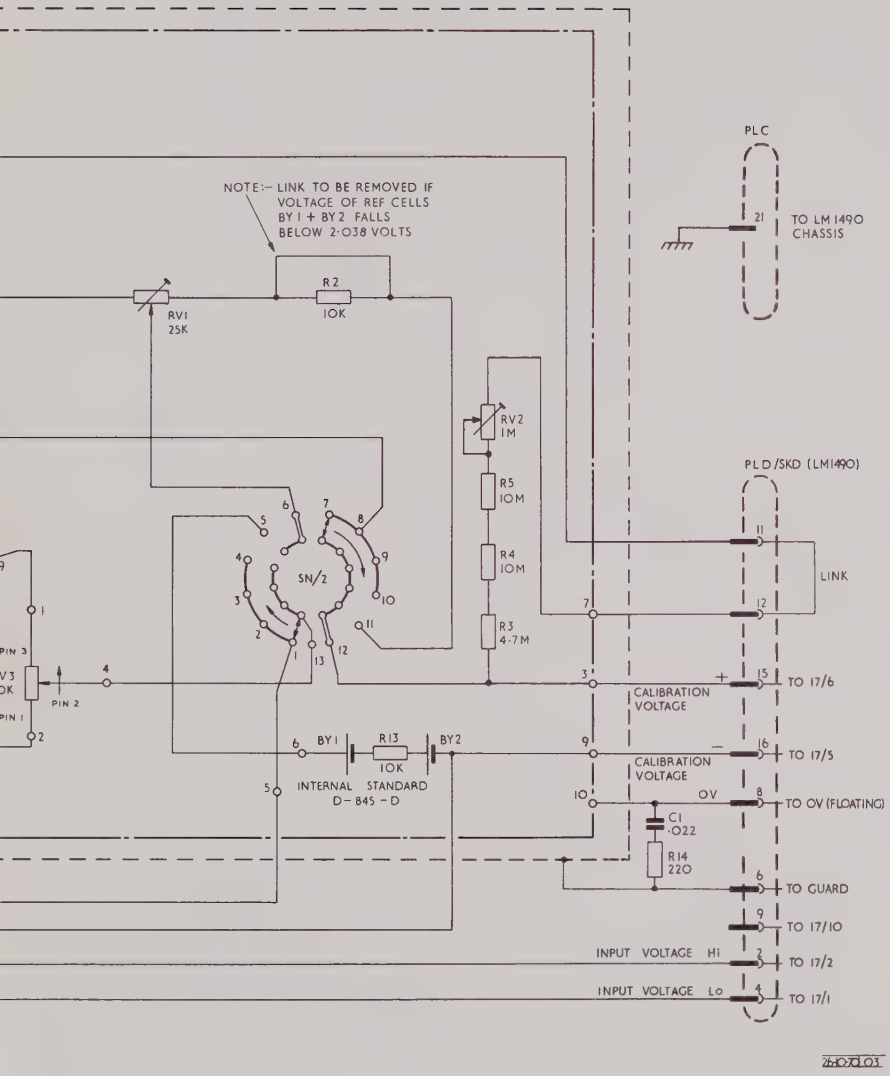
Cct. Ref.		General Description			Solartron Part No.
R1	V	68k	¼W	1%	198346802
R2	V	10k	¼W	1%	198341002
R3	V	4.7M	½W	1%	198664702
R4	V	10M	1W	1%	198971002
R5	V	10M	1W	1%	198971002
R6 to R10	V	25k	¼W	0.2%	A14920030
R13	V	25k	¼W	0.2%	A14920030
RV1		25k	1W	5%	122042500
RV2		1M	¾W	20%	124061000
RV3		50k	1.5W	1%	B14920031
BY1 to BY3		Cell Ref. D-845-D			310010010

EXTERNAL CALIBRATION UNIT EX1492

Cct. Ref.		General Description			Solartron Part No.
R11	X	10	1/8W	10%	172011000
R12	X	10	1/8W	10%	172011000
R14	X	220	1/8W	10%	172022200
C1	B	.022	160V	10%	220342200
PLC		Conn. Plug 24 Way			352324120
PLD		Plug Fixed 16 Way			352316080
SKF		Conn. Fixed			352803010
SKG		Conn. Fixed			352803010
		Terminal, Insulated, Red			355100510
		Terminal, Insulated, Black			355100500




REFERENCE CELL D-845
SKG
REAR PANEL INPUT
VIEW FROM REAR OF INSTRUMENT
Hi
Lo
G
R12
2·2K
8
BY3
R1
68K
SWITCH N
INTERNAL STANDARD
8
7
6
5
2
0
3
VOLTS
R6
R7
R8
R9
R10
25K
25K
25K
25K
25K
6
7
5
4
SN/1
3
2
1
13
SK F
FRONT PANEL INPUT
VIEW FROM FRONT OF INSTRUMENT
Hi
Lo
G
R11
2·2K
P C BOARD 1492910!
SCREENING BOX
+
EXTERNAL STANDARD
–


NOTE:– LINK TO BE REMOVED IF VOLTAGE OF REF CELLS BY 1 + BY 2 FALLS BELOW 2·038 VOLTS
RV1 25K
R2 10K
RV2 1M
R5 10M
R4 10M
R3 4·7M
SN/2
BY1
R13 10K
BY2
INTERNAL STANDARD D–845–D
PLC
21
TO LM 1490 CHASSIS
PLD/SKD (LM1490)
11
LINK
12
7
3
+
15
TO 17/6
CALIBRATION VOLTAGE
9
–
16
TO 17/5
CALIBRATION VOLTAGE
10
OV
8
TO OV (FLOATING)
C1 ·022
R14 220
6
TO GUARD
9
TO 17/10
INPUT VOLTAGE Hi
2
TO 17/2
INPUT VOLTAGE Lo
4
TO 17/1
PIN 3
PIN 2
PIN 1
2600103

EX1493 ZENER REFERENCE UNIT

This unit contains a Zener Diode stabilised voltage reference, and is used in place of the EX1491 DC unit. The advantages of this unit are that it has a better temperature coefficient (1ppm/^{o}C) and it is not sensitive to mechanical shock. The unit is fitted in the standard sub-unit location on the right-hand side of the LM1490.

SPECIFICATION

Reference:	'Julie' zener reference unit ZVR506.
Stability:	25ppm per 6 months
Temperature Coefficient:	$\pm$ 1ppm^{o}/C for 0 - 50^{o}C

CIRCUIT DESCRIPTION

The circuit is shown on diagram C14997000. Power is taken from the Flux Oscillator (Position 16) via T1. The full wave rectifier MR1/MR2 provides a +22V supply.

Potential Divider R3/R4/R5 reduces the Reference output (+6.3V) to +2.039V ($\equiv$ 2 standard cells). R6, RV1 and R7 provide adjustment of the output voltage by $\pm$ 400μV.

SETTING UP PROCEDURE

Apparatus Required:

As listed for the LM1490 Setting Up Procedure.

1. Plug the EX1493 into a fully tested LM1490.
2. Measure the voltage and ripple at TP1 with respect to TP4.

   Voltage : +22V $\pm$ 2V

   Ripple : <1mV p-p.
3. Select AUTO, 200ms and the 2V Range.

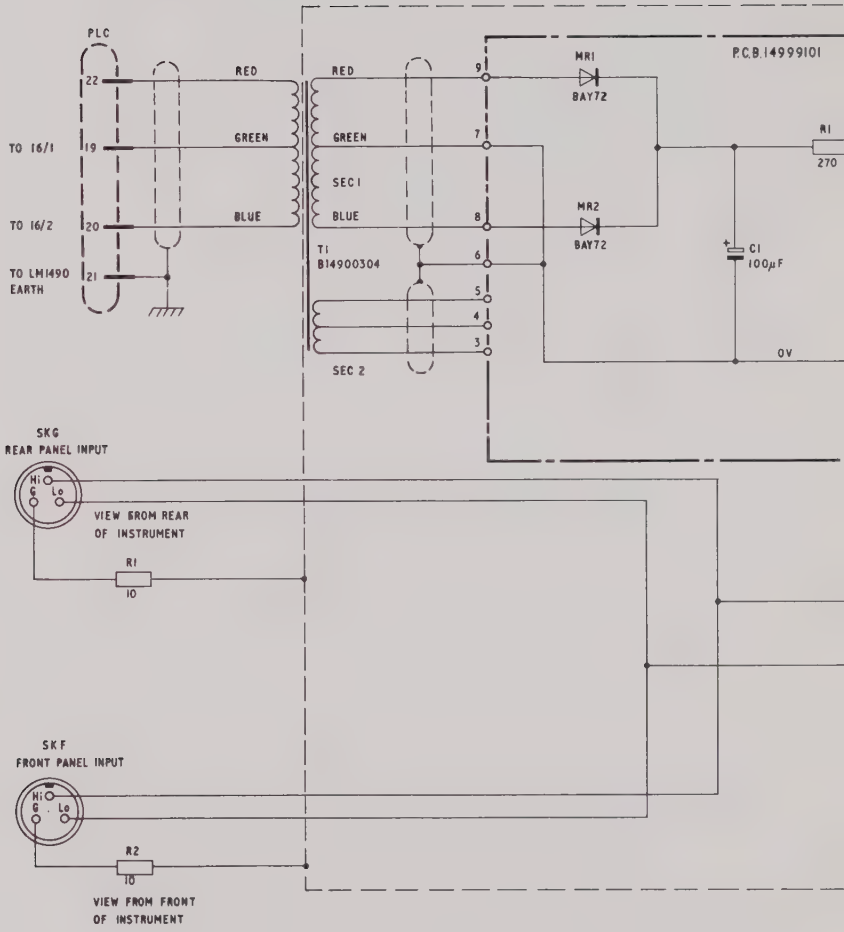
   Apply an input of -2.03900V using the dc potentiometer (at 20^{o}C). Repeatedly press CHECK CAL and adjust RV1 until a reading of -2.03900V is obtained.
4. Recheck the ac and dc common mode rejection of the LM1490 as per the Performance Checks on page 4.10.

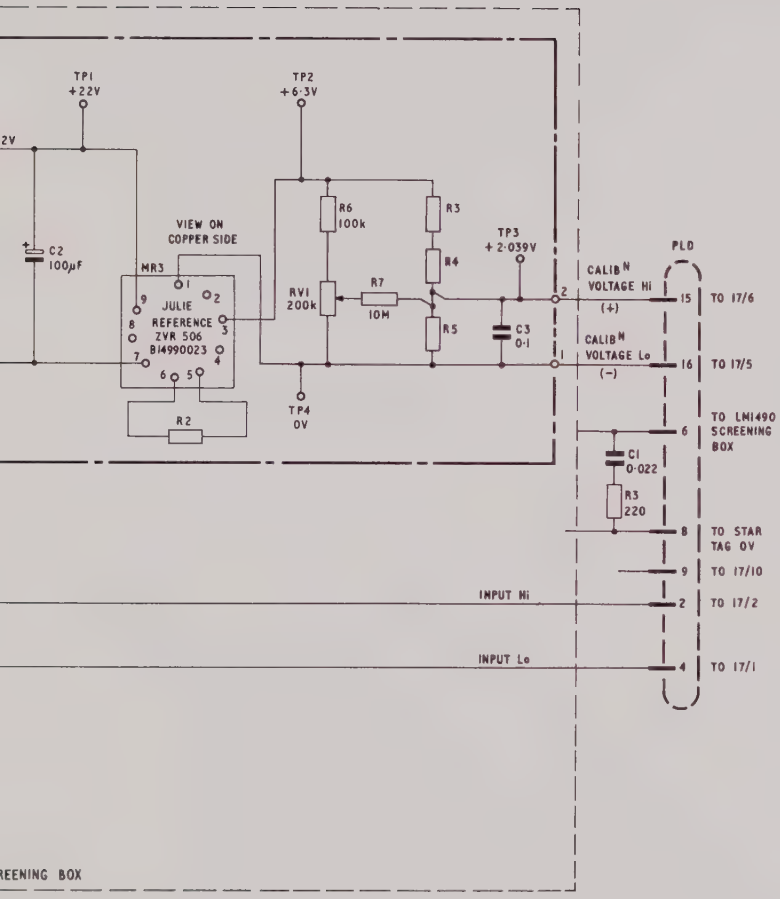
MAIN FRAME

Cct. Ref.	General Description				Solartron Part No.
R1	X	10	1/8W	$\pm$10%	172011000
R2	X	10	1/8W	$\pm$10%	172011000
R3	X	220	1/8W	$\pm$10%	172322200
C1	B	.022	160V	$\pm$10%	220342200
T1	Inverter Transformer				B14900334
PLC	24 Way Plug				352324120
PLD	16 Way Plug				352316080
SKF	Input Socket (front)				352803010
SKG	Input Socket (rear)				352803010

BOARD 1

Cct. Ref.	General Description				Solartron Part No.
R1	Z	270	½W	$\pm$1%	195422700
R6	V	100k	1/8W	$\pm$1%	191251002
R7	V	10M	1W	$\pm$1%	198971003
RV1	Multi-turn Cermet	200k	¾W	$\pm$30%	124052000
C1	J	100	35V	-20% +50%	208600127
C2	J	100	35V	-20% +50%	208600127
C3	Poly-ester Rect.	0.1	100V	$\pm$10%	225451000
MR3, R2, R3, R4, R5	Zener Reference ZVR506 and 4 selected Resistors				B14990023
MR1	BAY72				300524530
MR2	BAY72				300524530


PLC
22
19
20
21
RED
GREEN
BLUE
TO 16/1
TO 16/2
TO LM1490
EARTH
RED
GREEN
BLUE
SEC 1
SEC 2
T1
B14900304
9
7
8
6
5
4
3
MR1
BAY72
MR2
BAY72
P.C.B. 14999101
R1
270
C1
100μF
0V
SKG
REAR PANEL INPUT
Hi
G
Lo
VIEW FROM REAR
OF INSTRUMENT
R1
10
SKF
FRONT PANEL INPUT
Hi
G
Lo
R2
10
VIEW FROM FRONT
OF INSTRUMENT


TP1
+22V
TP2
+6·3V
2V
C2
100μF
VIEW ON
COPPER SIDE
MR3
JULIE
REFERENCE
ZVR 506
B14990023
R6
100k
R3
R4
RV1
200k
R7
10M
R5
TP3
+2·039V
C3
0·1
TP4
0V
R2
PLD
CALIB^N
VOLTAGE Hi
(+)
CALIB^N
VOLTAGE Lo
(-)
15
TO 17/6
16
TO 17/5
6
TO LN1490
SCREENING
BOX
C1
0·022
R3
220
8
TO STAR
TAG 0V
9
TO 17/10
INPUT Hi
2
TO 17/2
INPUT Lo
4
TO 17/1
REENING BOX

EX 1494 MULTIMETER UNIT

This unit is used to adapt the LM1490 for ac and resistance as well as dc measurements. It is fitted in the standard sub-unit location on the right-hand side of the LM1490. The calibration facility of the EX1491 is retained. The dc, ac and resistance ranges may be remotely programmed.

OPERATING INSTRUCTIONS

DC Ranges

The EX1494 Range Selector is set to DC RANGES.

The LM1490 Range Selector is set to the appropriate range or AUTO RANGE.

AC Ranges

The LM1490 Range Selector is set to SUB-UNIT.

The EX1494 Range Selector is set to the appropriate range. For frequencies less than 100Hz EXTEND LF RESPONSE should be selected.

Resistance Ranges

The LM1490 Range Selector is set to SUB-UNIT.

The EX1494 Range Selector is set to the appropriate range.

Remote Programming

The LM1490 Range Selector is set to SUB-UNIT.

The EX1494 Range Selector is set to PROGRAM.

Range, Mode and Extend LF Response are then programmed via SKA on the rear panel of the EX1494.

SKA Details

Input: DTL and TTL Compatable

$2V < \text{Logic } 1 < 5.5V$ at $< 1mA$

$-0.5V < \text{Logic } 0 < 0.8V$ at $< -1.6mA$

0V is connected to Pin H.

Mode

Mode	Pin A	Pin E
DC	1	0
AC	1	1
Ω	0	0
	Non-standard	
AC	0	1

Filter

Extend LF Response	Pin F
No	0
Yes	1

Fanout Unit EX1488

If the Fanout Unit EX1488 is used in conjunction with the LM1490 and EX1494 the remote programming and output information facilities of this unit are retained.

Range

Range	DC Range	AC Range	Resistance Range	Pin D (1)	Pin C (2)	Pin B (4)
1	20mV	–	–	1	0	0
2	200mV	200mV	2kΩ	0	1	0
3	2V	2V	20kΩ	1	1	0
4	20V	20V	200kΩ	0	0	1
5	200V	200V	2MΩ	1	0	1
6	*	1000V	20MΩ	0	1	1

* The 1000V dc range cannot be remotely programmed

SPECIFICATION

DC Measurement

As LM1490.

AC Measurement

Ranges

Range	Sensitivity	* Input Impedance	Max. Input (peak)
200.000mV	1μV	10MΩ/100pF	300V
2.00000V	10μV	10MΩ/100pF	300V
20.0000V	100μV	1MΩ/100pF	1000V
200.000V	1mV	1MΩ/100pF	1000V
1000.00V	10mV	1MΩ/100pF	1000V

*Input Capacitance not including input cable.

Characteristics

Range	Accuracy over 90 days ± 5°C		Temperature Coefficient per °C
	40Hz to 20kHz	20Hz to 100kHz Typically	
200.00mV	0.05% Reading ±0.015%fs	1% Reading ±0.015%fs	0.002%
2.00000V	0.05% Reading ±0.015%fs	1% Reading ±0.015%fs	0.002%
20.0000V	0.1% Reading ±0.015%fs	1% Reading ±0.015%fs	0.01%
200.000V	0.1% Reading ±0.015%fs	1% Reading ±0.015%fs	0.01%
1000.00V	0.1% Reading ±0.015%fs	1% Reading ±0.015%fs	0.01%

EXTEND LF RESPONSE must be selected for measurements at less than 100Hz.

The values given above are for a scale length of 250 000. If a shorter scale is chosen the accuracy will be degraded by an additional ±1 digit in the last decade displayed.

Settling Time:

< 1s. to 0.1% of reading. This increases to < 8s. if EXTEND LF RESPONSE is selected.

Overload Recovery:

< 4s. provided EXTEND LF RESPONSE is not selected.

Common Mode Rejection:

> 140dB at DC

> 40dB at 50Hz

Series Mode Rejection:

> 120dB at DC.

Resistance Measurement

Ranges

Range	Sensitivity	Test Current	Max. Input (peak)
2.00000kΩ	10mΩ	1mA	300V
20.0000kΩ	100mΩ	1mA	300V
200.000kΩ	1Ω	10μA	300V
2.00000MΩ	10Ω	10μA	300V
20.0000MΩ	100Ω	1μA	300V

Characteristics

Range	Accuracy over 90 days ± 5°C	Temperature Coefficient per °C
2.00000kΩ	0.03% Reading ± 0.001% fs	0.004%
20.0000kΩ	0.03% Reading ± 0.001% fs	0.004%
200.000kΩ	0.03% Reading ± 0.001% fs	0.004%
2.00000MΩ	0.03% Reading ± 0.001% fs	0.004%
20.0000MΩ	0.25% Reading ± 0.001% fs	0.005%

The values given above are for a scale length of 250 000. If a shorter scale is chosen the accuracy will be degraded by an additional ± 1 digit in the last decade displayed.

Series Mode Rejection:

As for dc measurement.

Input:

Fully floating four terminal measurement.

CIRCUIT DESCRIPTION

Logic, Board 1

Table 1 : Mode Logic

Mode	Program Mode Cmd		OR	Switch Range Lines				Relays Energised	
	$\overline{\Omega}$ Pin A	AC Pin E		1	9	5	6	RLP	RLQ RLR
DC Rem	1	0							
AC	1	1		*	1	0	0		+
Ω	0	0		*	1	1	1	+	
AC	0	1		*	-	-	-		+
DC Local	-	-		*	0	0	1		

*Switch line 1 is at 0 only when PROGRAM is selected.

Table 2 : Range Logic

Mode	Range	Program Range Cmd. '4' Pin B	'2' Pin C	'1' Pin D	OR Switch Range Lines 2	3	4	Relays Energised RLG	RLH	RLJ	LM1490 RANGE	Decimal Points Called DP1	DP2	DP3	DP4	Units Called V	mV
DC Remote	20mV	0	0	0				+	+	+	20mV		+				+
	20mV	0	0	1				+	+	+	20mV		+				+
	200mV	0	1	0				+		+	200mV			+			+
	2V	0	1	1	All high			+			2V	+				+	
	20V	1	0	0					+	+	20V		+			+	
	200V	1	0	1					+		200V			+		+	
	200V	1	1	0							-					+	
	200V	1	1	1							-					+	
DC Local					All high						As Selected						
AC	200mV	0	0	0				+	+	+	2V			+			+
	200mV	0	0	1				+	+	+	2V			+			+
	200mV	0	1	0	1	0	1	+		+	2V			+			+
	2V	0	1	1	1	0	0	+			2V	+				+	
	20V	1	0	0	0	1	1		+	+	2V		+			+	
	200V	1	0	1	0	1	0		+		2V			+		+	
	1kV	1	1	0	0	0	1				2V				+	+	
	1kV	1	1	1							2V				+	+	
OHMS	2kΩ	0	0	0				+	+	+	2V	+					
	2kΩ	0	0	1				+	+	+	2V	+					
	2kΩ	0	1	0	1	0	1	+		+	2V	+					
	20kΩ	0	1	1	1	0	0	+			20V		+				
	200kΩ	1	0	0	0	1	1		+	+	2V			+			
	2MΩ	1	0	1	0	1	0		+		20V	+					
	20MΩ	1	1	0	0	0	1				20V			+			
	20MΩ	1	1	1							20V			+			

AC Attenuator, Board 2

Potential dividers provide 100 : 1 and 1000 : 1 attenuation. C4 and C5 are adjusted to maintain correct attenuation at high frequencies.

AC Range	Attenuation	RLG Energised	RLH Energised
200mV	1 : 1	Yes	No
2V	1 : 1	Yes	No
20V	100 : 1	No	Yes
200V	100 : 1	No	Yes
1000V	1000 : 1	No	No

EX1494 Calibrator, Board 5

Provides a calibration voltage from standard cells for the LM1490. RV1 gives fine adjustment of the calibration voltage (± 1mV).

Ohms Unit, Board 4

The output of T1 is rectified to give a ±22V isolated floating supply to the AC Converter (Board 3) and the Ohms Unit.

The constant current to the Reference zener Diode MR8 from VT3 is set by MR9, MR10 and R7 to approximately 7.5mA. The Reference voltage at TP1 (approximately 8.2V) is set by potential divided R3 and R8 to R16 and adjusted by the links and RV1. MR8 also sets the constant current to MR9/MR10 via VT4 and R17.

Differential amplifier VT6 and IC1 compares the reference voltage with the voltage across the reference resistors selected by RLG2 and RLH2 and adjusts the current through VT7 so that the voltages are always equal. This current is used as the test current through the resistor being measured.

Constant current source VT5 sets the total source current of VT6 to approximately 60μA.

AC Converter, Board 3

VT1, IC1, VT3 and VT4 are a high gain differential amplifier. C4 provides an ac bypass channel to maintain gain at high frequencies.

RLJ2 contacts when closed (200mV and 20V ranges) increase the gain of VT4 to maintain the frequency response when the ac feedback to TR16 is decreased.

Low pass filters R29/C13/R33/C17/R35/C19 and R31/C14/R34/C18/R3/C20 average the positive and negative half cycle outputs respectively of the VT5/VT6 output stage (via MR14 and MR15). This generates a differential output between H15 and LO5 proportional to mean-modulus of the ac input voltage. This output is scaled by potential dividers, selected by RLJ1 contacts connected as ac feedback around the converter so that the instrument indicates rms values. The fsd (input equal to range) differential output is 2V on all ranges except the 1000V range, when it is limited to 1V by the maximum permitted input.

DC feedback via R13 stabilises the dc operating point of the AC Converter, set by RV3.

When an extended low frequency response is required switch SB causes RLF to be energised. This increases the time constant of the low pass filters and enables steady readings to be made at frequencies of less than 100Hz.

AC Range	Input Attenuation	RLJ energised	DC fsd output
200mV	1 : 1	Yes	2V
2V	1 : 1	No	2V
20V	100 : 1	Yes	2V
200V	100 : 1	No	2V
1000V	1000 : 1	No	1V

Resistance Range	RLG Energised	RLH Energised	Test Current	LM1490 DC Range
2kΩ	Yes	No	1mA	2V
20kΩ	Yes	No	1mA	20V
200kΩ	No	Yes	10μA	2V
2MΩ	No	Yes	10μA	20V
20MΩ	No	No	1μA	20V

SETTING UP PROCEDURE

Apparatus Required

As listed for the LM 1490 setting Up Procedure plus

AC Calibrator Accuracy ±0.02% (e.g. Hewlett Packard 745A with the High Voltage Amplifier 746A).

Ω Calibrator Accuracy ±0.005% (e.g. Dekastat RS624A checked to ±0.005%).

10MΩ Wirewound resistor, of known value to better than 0.01% at 20°C.

20MΩ Wirewound resistor, of known value to better than 0.05% at 20°C.

Plug the module into a fully tested LM1490. The LM1490 must contain the 'Inverter version' of PCB 16.

1. Rail Checks

Adjust RV1 Pos'n 1 on the LM1490 to make the +18V rail (measured at Pos'n 18) in the floating unit 18.2V. Check the ± 22V rails and ripples on PCB 4 of the EX1494.

Rails: 22V ± 1V

Ripple: ⩾ 10mV p-p measured across C3 and C4 pcb 4.

2. Display Indicator Checks

On the LM1490 select AUTO, 200mS

a) Switch the EX1494 to DC. Check at TP1, 2 and 3 on PCB 1 of the module that the enable lines are all at 0V. ± 1V.

b) Ensure all the dc ranges on the LM1490 can be called up with correct decimal point positions. Check also the mV and V signs.

c) Switch the LM1490 to SUB-UNIT and check the correct decimal point positions are indicated on all ac and Ω ranges.

d) Check the decimal points and V and mV signs on the ac ranges.

e) Check the decimal point indicators on the Ω ranges (V and mV should not be lit).

3. Remote Checks

a) Switch the EX1494 to PROGRAM. The ~ sign should be lit.

b) Connect pins A and E of socket 'A' to 0V. The mV and V signs should not be lit.

c) Connect pin E to 0V and check that all the dc ranges 20mV to 200V can be commanded remotely on pins B, C and D of SKTA as shown in the table.

0 = 0V 1 = pin O/C

Range	Pin B	Pin C	Pin D	Range Called
1	0	0	0/1	20mV
2	0	1	0	200mV
3	0	1	1	2V
4	1	0	0	20V
5	1	0	1	200V

4. DC Tests

a) Switch the EX1494 to DC. Set the LM1490 to the 2V range. Apply -2.00000V to the input and adjust RV1 on PCB 5 of the EX1494 for a reading of -2.00000V. It will be necessary to press the CHECK CAL button after each adjustment of RV1.

b) Recheck the ac and dc common mode rejection of the LM1490 as per the Performance Checks 8 and 9 on page 4.10.

5. Ohms Tests

Select 200mS, LINE SYNC., AUTO, SUB-UNIT.

a) Switch the EX1494 to the 2kΩ range and connect an external resistance of known value near 2kΩ. Adjust RV1 on PCB 4 to obtain a display reading equal to the value of the external resistance.

b) Change the resistance to one of value near to 20kΩ and the range to 20kΩ. The display should indicate the value of the resistance ± 5 digits.

c) Change the resistance to one of value near to 20MΩ and the range to 20MΩ. Adjust RV2 PCB 4 until the display indicates the value of resistance.

d) Change the resistance to one of value near to 200kΩ and the range to 200kΩ. Adjust RV3 PCB 4 until the display indicates the value of the resistance.

e) Change the resistance to one of value near to 2MΩ and the range to 2MΩ. The display should indicate the value of the resistance ± 5 digits.

Note: If MR8 on PCB 4 is replaced, the link pattern of this board may need adjustment. Consult Solartron for details.

6. AC Tests

Select 20mS, LINE SYNC, AUTO, SUB-UNIT.

a) Short circuit the input leads and check on the ac ranges 200mV to 1000V the reading does not exceed 3 digits. Allow a short time for the reading to run down to zero.

b) Using the AC Calibrator 745A feed in 2.0000V at 1kHz on the 2V range and adjust RV2 PCB 3 for a reading of 2.0000V. Reduce the input to 0.2000V and adjust RV3 PCB 3 for a reading of 0.2000V.

c) Feed in the voltages at 1kHz as shown in the table, adjusting the potentiometers and checking the readings.

Range	AC Input	Adjustments	Reading
2V	2.0000V	RV2 PCB 3	2.0000V
200mV	200.00mV	RV1 PCB 3	200.00mV
20V	20.000V	RV1 PCB 2	20.000V
200V*	200.00V	—	200.00 ±.02V
1000V*	800.0V	RV2 PCB 2	800.0V

*For these ranges the High Voltage Amplifier 746A is required.

7. Final Calibration at 20°C

DC Calibration

Carry out the procedure as detailed in the LM1490 setting up Procedure from page 4.12. If the LM1490 has been previously calibrated at this stage it will be necessary to carry out the Internal Standard section, adjusting RV1 on EX1494 PCB 5, and then recheck the accuracy on all ranges.

Ohms Calibration

Select 200mS, LINE SYN, AUTO, SUB-UNIT.

Check out the ohms ranges 2kΩ to 20MΩ with the resistance values shown in the table making adjustments to the potentiometers as necessary until the display reading equals the resistance value.

OHMS Range	Approximate External Resistor	Adjustments	Limits
2kΩ	2.00000k	RV1 PCB 4	±5 digits
	1.50000k	—	±4 digits
	1.00000k	—	±3 digits
	0.50000k	—	±2 digits
20kΩ	20.0000k	RV1 PCB 4	±5 digits
	15.0000k	—	±4 digits
	10.0000k	—	±3 digits
	5.0000k	—	±2 digits
200kΩ	200.000k	RV3 PCB 4	±5 digits
	150.000k	—	±4 digits
	100.000k	—	±3 digits
	50.000k	—	±2 digits
2MΩ	2.00000M	—	±10 digits
	1.50000M	—	±8 digits
	1.00000M	—	±6 digits
	0.50000M	—	±3 digits
20MΩ	10.0000M	RV2 PCB 4	±5 digits
	20.0000M	—	±100 digits

AC Calibration

Select 20mS, LINE SYNC, AUTO, SUB-UNIT

a) Using the AC Calibrator 745A, feed in the following voltages at 1kHz on the 200mV and 2V ac ranges.

Make adjustments to the potentiometers where necessary and check the readings are within the specified limits.

AC Range	AC Input	Adjustments	Limits
2V	2.0000V	RV2 PCB 3	—
	1.5000V	—	±1 digit
	1.0000V	—	±1 digit
	0.5000V	—	±1 digit
200mV	200.00mV	RV1 PCB 3	—
	150.00mV	—	±1 digit
	100.00mV	—	±1 digit
	50.00mV	—	±1 digit

b) Feed in 20.000V at 20kHz on the 20V range and adjust C4 PCB 2 for a reading of 20.000V.

c) Change the frequency to 1kHz and adjust RV1 PCB 2 for a reading of 20.000V.

d) Repeat (b) and (c) until both readings are correct.

e) Feed in 1000V at 20kHz on the 1000V range and adjust C5 PCB 2 for a reading of 1000.0V. (Use the High Voltage Amplifier 746A).

f) Change the frequency to 1kHz and adjust RV2 PCB 2 for a reading of 1000.0V.

g) Repeat (e) and (f) until both readings are correct.

h) Feed in the following voltages at 1kHz on the 20V to 1000V ac ranges checking the readings are within the specified limits.

AC Range	AC Input	Limits
20V	20.000V	—
	15.000V	± 1 digit
	10.000V	± 1 digit
	5.000V	± 1 digit
200V	200.00V	± 2 digits
	150.00V	± 2 digits
	100.00V	± 1 digit
	50.00V	± 1 digit
1000V	1000.0V	—
	500.0V	± 1 digit
	200.0V	± 1 digit

Frequency Response Checks

Feed in the following voltages at the frequencies indicated checking the readings are within the specified limits. Select EXTEND LF RESPONSE for 40Hz checks.

Some final adjustment of C1 and C2 may be necessary on ranges 20V and 1000V to obtain the best overall frequency response.

It may be necessary to slightly change the setting of the linearity control RV3 PCB 3 in order to obtain the best performance between 1kHz and 20kHz at 10% of full scale readings.

AC Range	AC Input	Frequency	Limits
200mV	200.00mV	100kHz	± 150 digits
	20.00mV	100kHz	± 18 digits
	200.00mV	50kHz	± 75 digits
	200.00mV	20kHz	± 15 digits
	20.00mV	20kHz	± 4 digits
	200.00mV	10kHz	± 7 digits
	200.00mV	5kHz	± 3 digits
	200.00mV	2.5kHz	± 2 digits
	200.00mV	100Hz	± 6 digits
	200.00mV	40Hz	± 10 digits
2V	2.0000V	100kHz	± 150 digits
	0.2000V	100kHz	± 18 digits
	2.0000V	50kHz	± 75 digits
	2.0000V	20kHz	± 15 digits
	0.2000V	20kHz	± 4 digits
	2.0000V	10kHz	± 7 digits
	2.0000V	5kHz	± 3 digits
	2.0000V	2.5kHz	± 2 digits
	2.0000V	400Hz	± 5 digits
	2.0000V	40Hz	± 10 digits
20V	20.000V	100kHz	± 150 digits
	2.000V	100kHz	± 18 digits
	20.000V	50kHz	± 75 digits
	20.000V	20kHz	± 15 digits
	2.000V	20kHz	± 4 digits
	20.000V	10kHz	± 7 digits
	20.000V	5kHz	± 3 digits
	20.000V	2.5Hz	± 2 digits
	20.000V	100Hz	± 5 digits
	20.000V	40Hz	± 10 digits
200V	200.00V	100kHz	± 150 digits
	20.00V	100kHz	± 18 digits
	200.00V	50kHz	± 75 digits
	200.00V	20kHz	± 15 digits
	20.00V	20kHz	± 4 digits
	200.00V	10kHz	± 7 digits
	200.00V	5kHz	± 3 digits
	200.00V	2.5kHz	± 2 digits
	200.00V	400Hz	± 5 digits
	200.00V	40Hz	± 10 digits
1000V	200.0V	100kHz	± 18 digits
	1000.0V	50kHz	± 40 digits
	1000.0V	20kHz	± 8 digits
	200.0V	20kHz	± 4 digits
	1000.0V	10kHz	± 4 digits
	1000.0V	5kHz	± 4 digits
	1000.0V	2.5kHz	± 4 digits
	1000.0V	100Hz	± 4 digits
	1000.0V	40Hz	± 6 digits

ACCESSORIES

Input Lead	ADA2000168
26 Way Plug	354002370
Pins	354001610

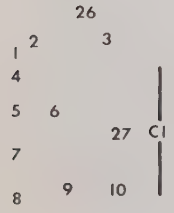
Note: The Solartron EX3183 5 Way Input Lead is suitable for this instrument

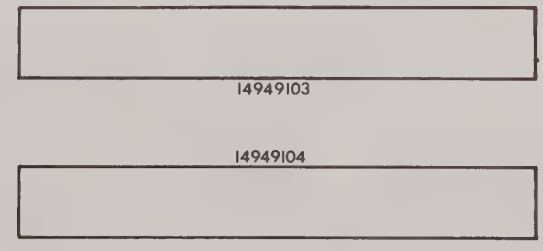
MAIN FRAME

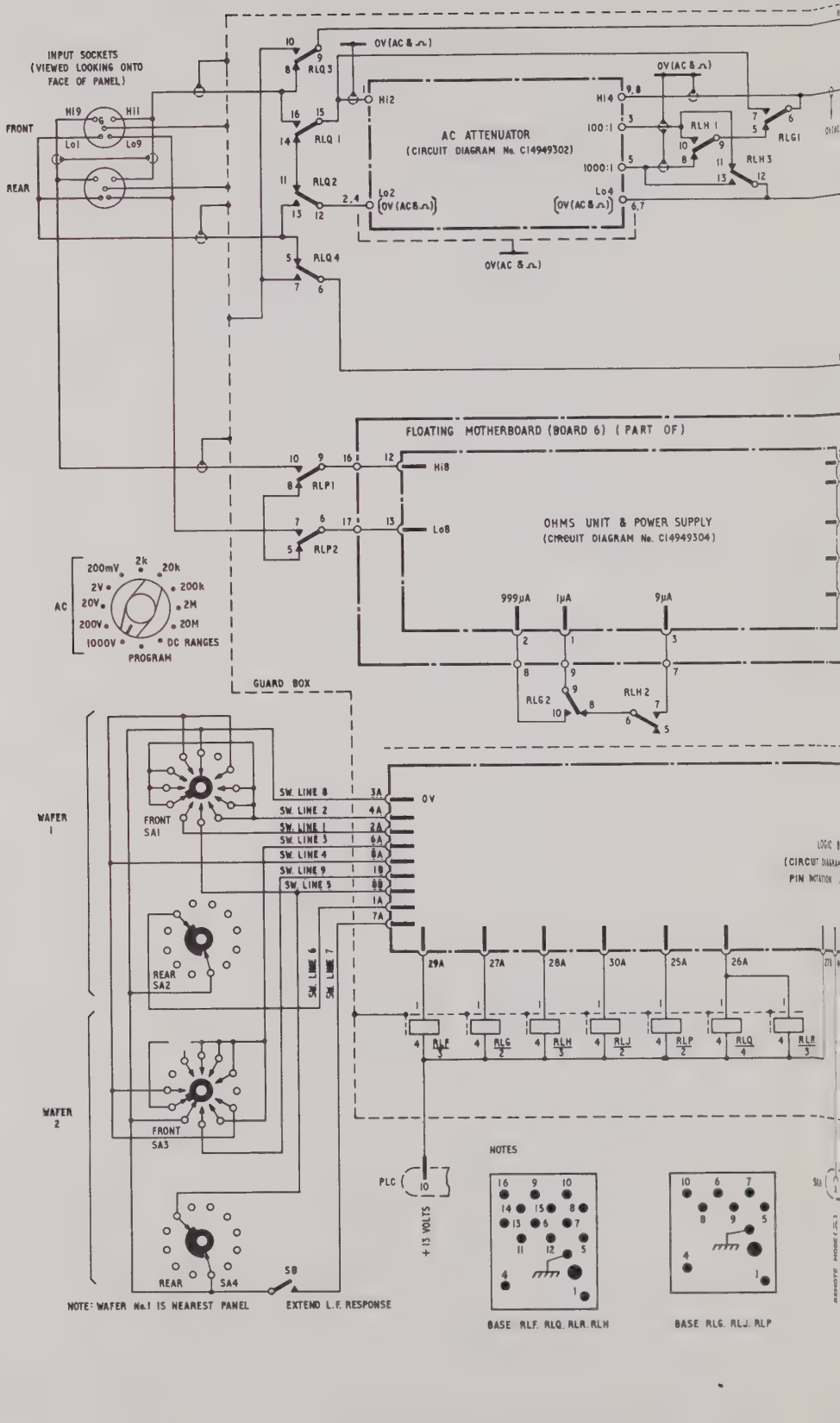
Cct. Ref.	General Description	Solartron Part No.
R3	X 220	172322200
C1	B 0.022 160V ±10%	220342200
C2	P 12p 1.5W	290060050
C3	A 8.2p 500V ±½p	208100089
SA	12 Way 3P Rotary Switch	379603001
SB	D.P.D.T. Push Button Switch	377000310
T1	Inverter Transformer	14900343
RLG	Relay 2P c/o	3012002
RLH	Relay 4P c/o	3012011
RLJ	Relay 4P c/o	3012002
RLP	Relay 4P c/o	3012002
RLQ	Relay 4P c/o	3012011
RLR	Relay 4P c/o	3012011
RLF	Relay 4P c/o	2012011
PLC	24 Way Plug	352324120
PLD	16 Way Plug	352316070
SK1	Input Socket (front)	352105010
SK2	Input Socket (rear)	352105010
SK3	26 Way Socket	354001260

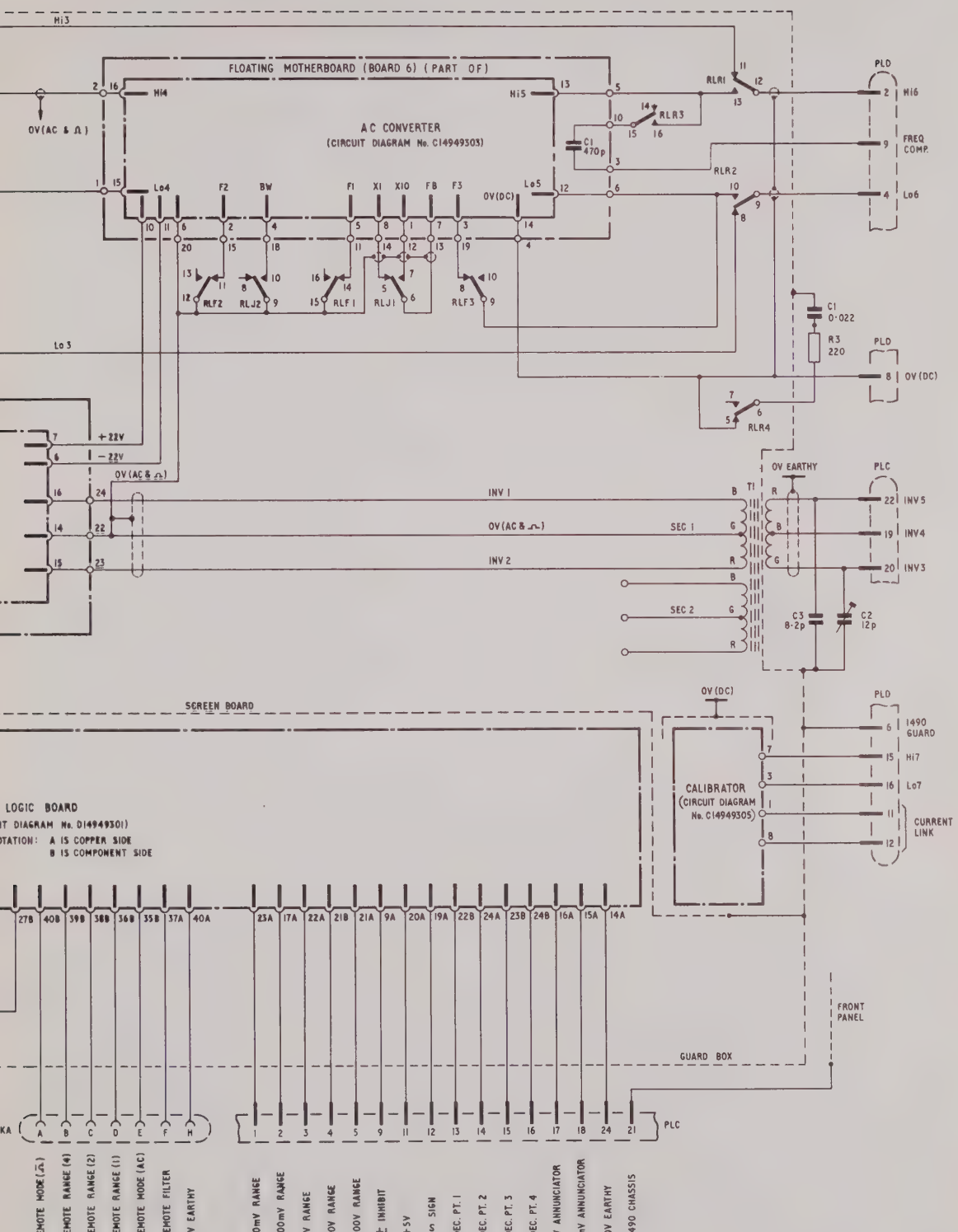
MOTHER BOARD

Cct. Ref.	General Description	Solartron Part No.
C1	B 470p 400V ± 10%	222324700
SK3	16 Way Socket	352516310
SK4	16 Way Socket	352516310





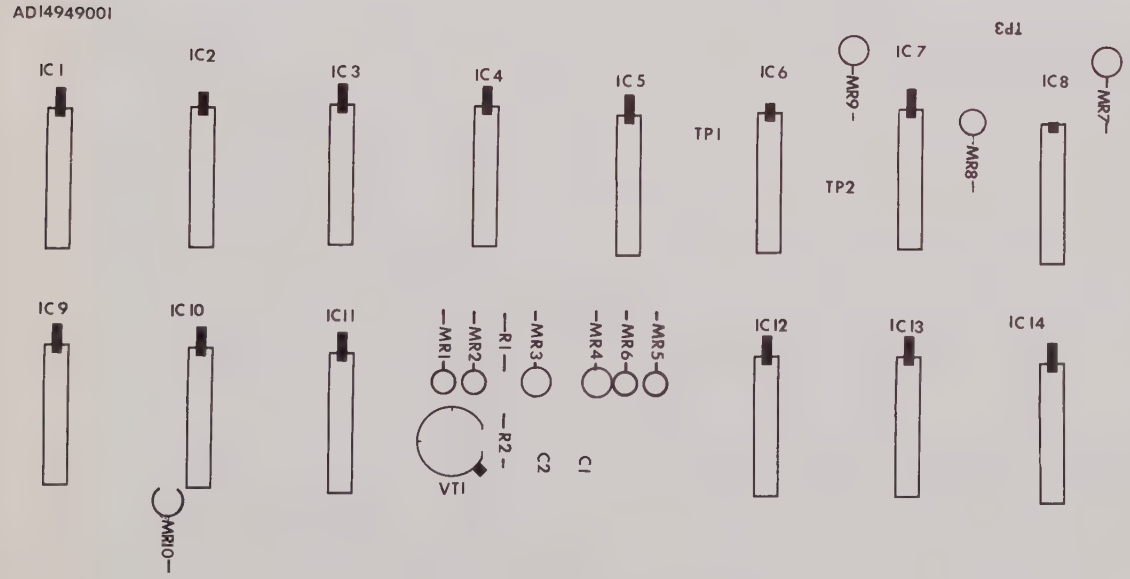

INPUT SOCKETS
(VIEWED LOOKING ONTO
FACE OF PANEL)
FRONT
REAR
Hi9
Hi1
Lo1
Lo9
RLQ3
RLQ1
RLQ2
RLQ4
Hi2
Lo2
0V(AC & Ω)
AC ATTENUATOR
(CIRCUIT DIAGRAM No. C14949302)
Hi4
100:1
1000:1
RLH1
RLH3
RLG1
Lo4
FLOATING MOTHERBOARD (BOARD 6) (PART OF)
RLP1
RLP2
Hi8
Lo8
OHMS UNIT & POWER SUPPLY
(CIRCUIT DIAGRAM No. C14949304)
999µA
1µA
9µA
RLG2
RLH2
AC
200mV
2V
20V
200V
1000V
2k
20k
200k
2M
20M
DC RANGES
PROGRAM
GUARD BOX
WAFER 1
WAFER 2
FRONT SA1
REAR SA2
FRONT SA3
REAR SA4
SW. LINE 8
SW. LINE 2
SW. LINE 1
SW. LINE 3
SW. LINE 4
SW. LINE 9
SW. LINE 5
SW. LINE 6
SW. LINE 7
0V
29A
27A
28A
30A
25A
26A
RLF
RLG/2
RLH/3
RLJ/2
RLP/2
RLQ/4
RLR/3
PLC
+13 VOLTS
S8
EXTEND L.F. RESPONSE
NOTES
BASE RLF. RLQ. RLR. RLH
BASE RLG. RLJ. RLP
NOTE: WAFER No.1 IS NEAREST PANEL

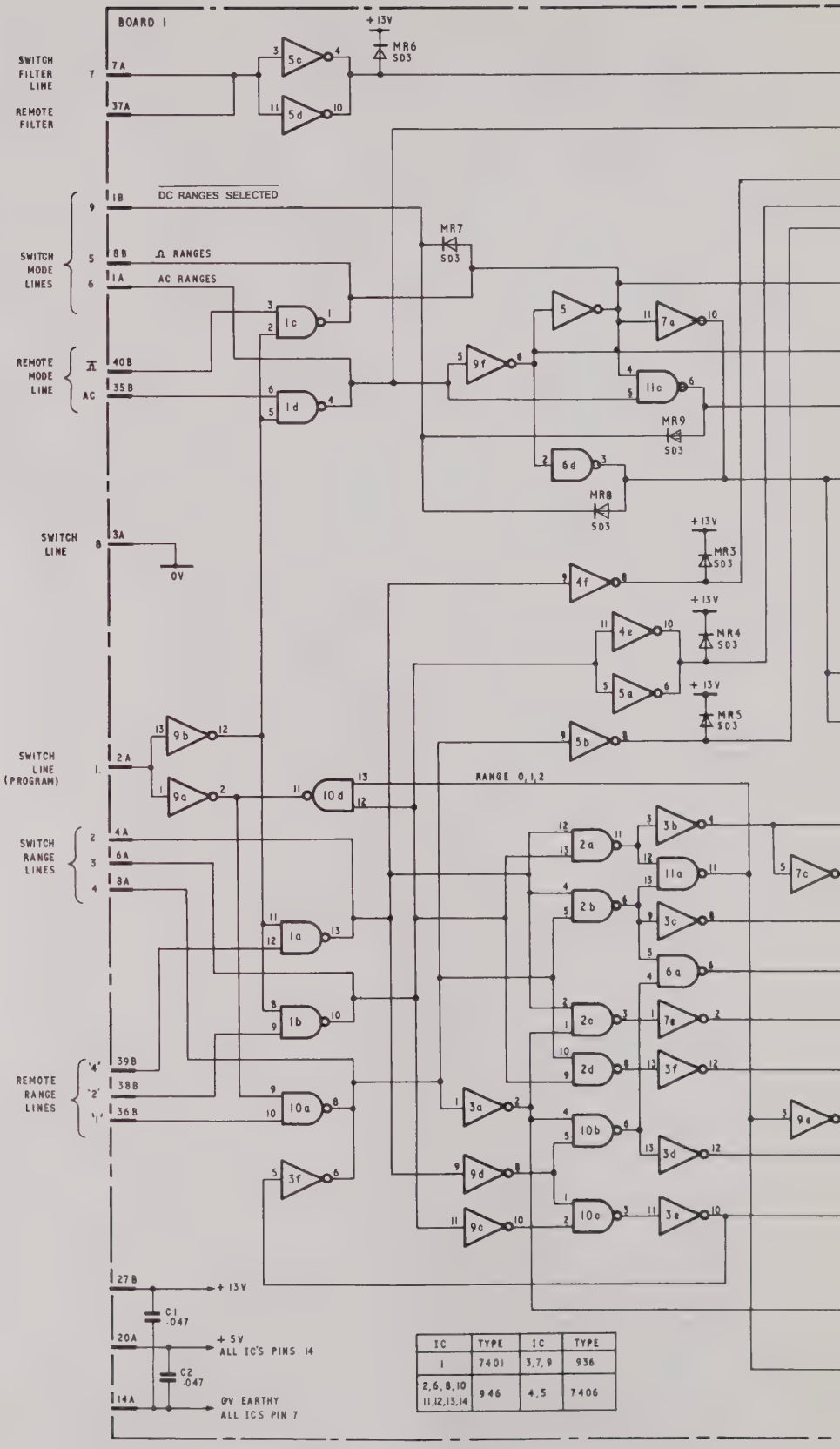

FLOATING MOTHERBOARD (BOARD 6) (PART OF)
AC CONVERTER
(CIRCUIT DIAGRAM No. C14949303)
Hi3
Hi4
Hi5
Lo4
Lo5
Lo6
Lo3
F1
F2
F3
XI
X10
FB
BW
OV(DC)
OV(AC & Ω)
RLR1
RLR2
RLR3
RLR4
RLF1
RLF2
RLF3
RLJ1
RLJ2
C1 470p
C1 0·022
R3 220
+22V
−22V
INV 1
INV 2
SEC 1
SEC 2
T1
OV EARTHY
PLD
PLC
Hi6
FREQ COMP.
OV(DC)
INV5
INV4
INV3
C3 8·2p
C2 12p
SCREEN BOARD
LOGIC BOARD
IT DIAGRAM No. D14949301)
OTATION: A IS COPPER SIDE
B IS COMPONENT SIDE
CALIBRATOR
(CIRCUIT DIAGRAM
No. C14949305)
1490 GUARD
Hi7
Lo7
CURRENT LINK
FRONT PANEL
GUARD BOX
27B 40B 39B 38B 36B 35B 37A 40A
23A 17A 22A 21B 21A 9A 20A 19A 22B 24A 23B 24B 16A 15A 14A
REMOTE MODE (Ω)
REMOTE RANGE (4)
REMOTE RANGE (2)
REMOTE RANGE (1)
REMOTE MODE (AC)
REMOTE FILTER
OV EARTHY
20mV RANGE
200mV RANGE
2V RANGE
20V RANGE
200V RANGE
± INHIBIT
+5V
± SIGN
DEC. PT. 1
DEC. PT. 2
DEC. PT. 3
DEC. PT. 4
V ANNUNCIATOR
mV ANNUNCIATOR
OV EARTHY
1490 CHASSIS

LOGIC, BOARD 1

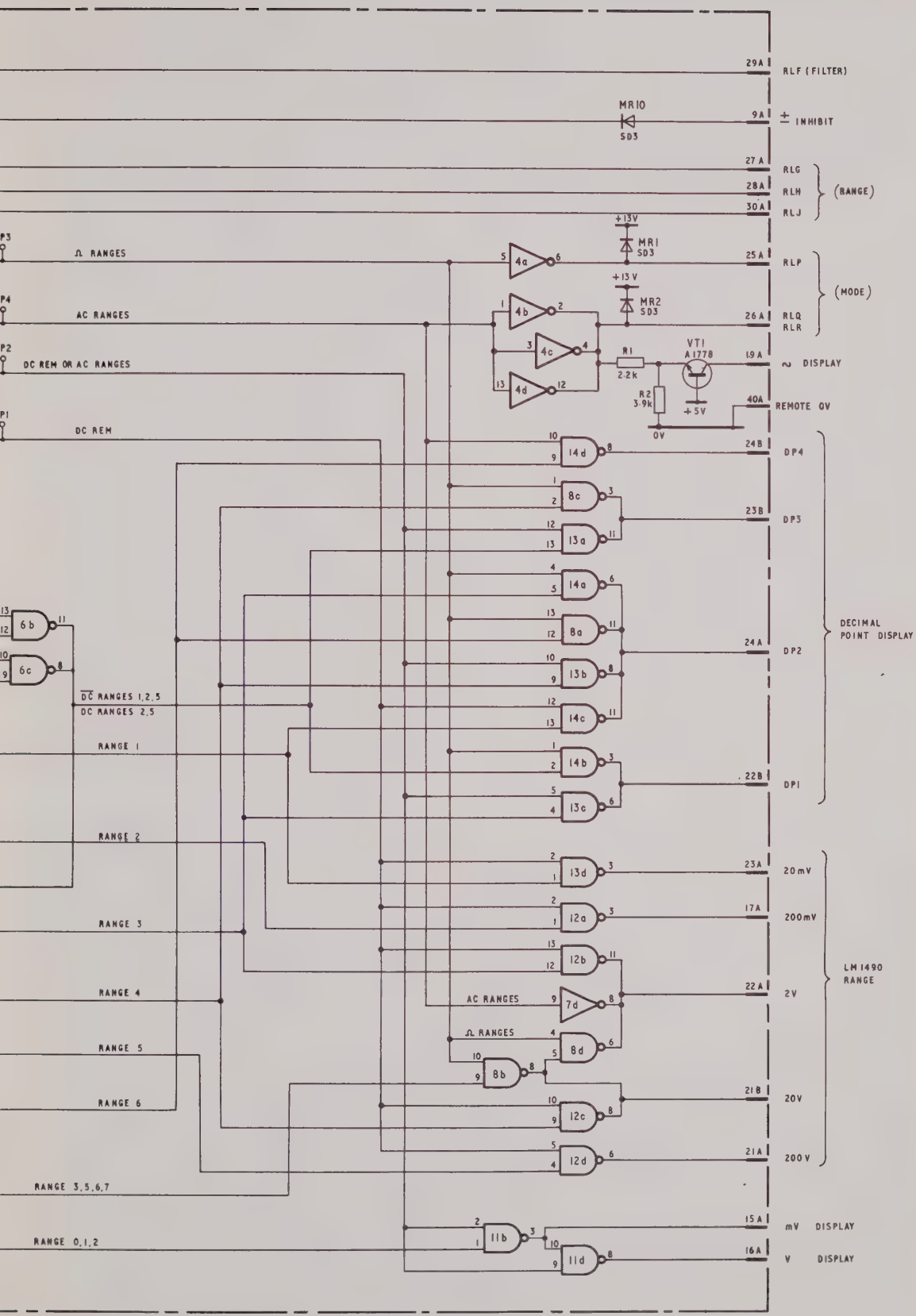
Cct. Ref.	General Description				Solartron Part No.
R1	X	2.2k	1/8W	10%	172032200
R2	X	3.9k	1/8W	10%	172033900
C1	G	0.047	25V	-20% +10%	241944700
C2	G	0.047	25V	-20% +10%	241944700
IC1	7401				510000400
IC2	946				510000160
IC3	936				510000290
IC4	7406				510000760
IC5	7406				510000760
IC6	946				510000160
IC7	936				510000290
IC8	946				510000160
IC9	936				510000290
IC10	946				510000160
IC11	946				510000160
IC12	946				510000160
IC13	946				510000160
IC14	946				510000160

Cct. Ref.	General Description	Solartron Part No.
VT1	A1778	300551430
MR1	SD3	300522160
MR2	SD3	300522160
MR3	SD3	300522160
MR4	SD3	300522160
MR5	SD3	300522160
MR6	SD3	300522160
MR7	SD3	300522160
MR8	SD3	300522160
MR9	SD3	300522160





IC	TYPE	IC	TYPE
1	7401	3,7,9	936
2,6,8,10 11,12,13,14	946	4,5	7406

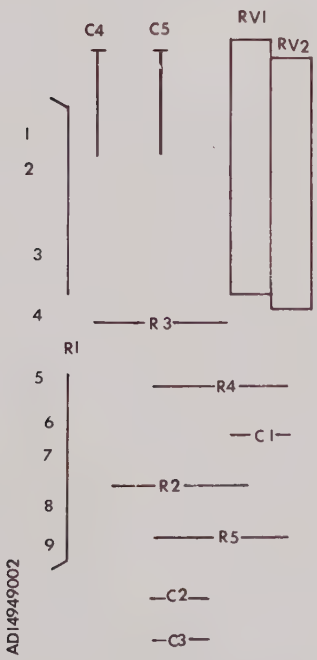


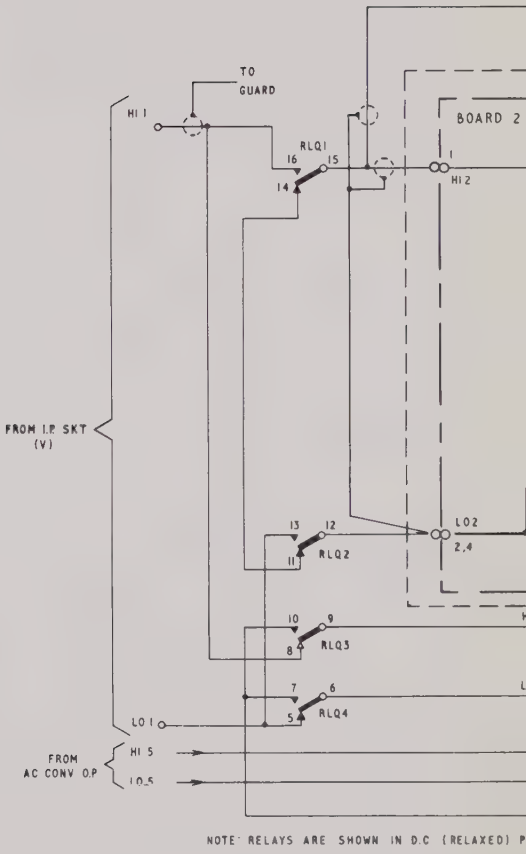
D14949301/01

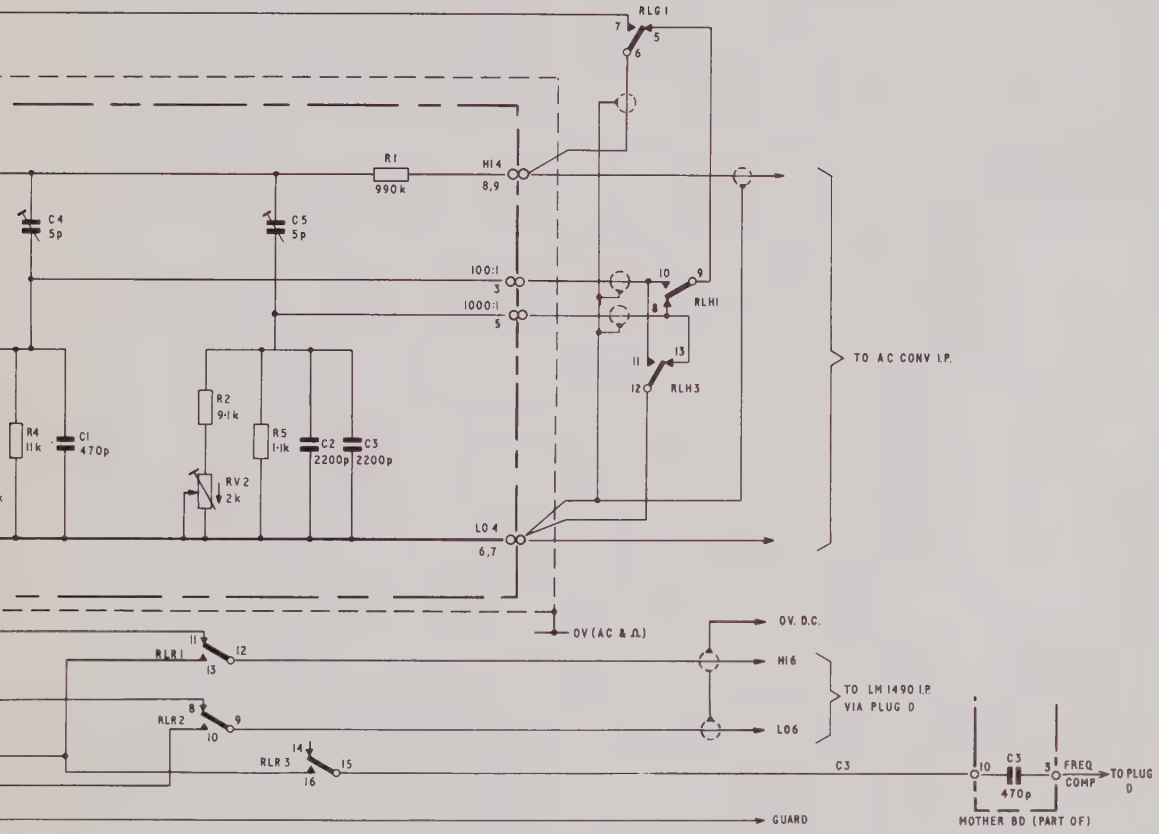
LOGIC, BOARD 1

AC ATTENUATOR, BOARD 2

Cct. Ref.		General Description			Solartron Part No.	Cct. Ref.		General Description			Solartron Part No.
R1	V	990k	2W	0.1%	169600501	C1	H	470p	350V	5%	250324700
R2	V	9.1k	¼W	1%	198339102	C2	H	2200p	350V	5%	250332200
R3	V	100k	¼W	1%	198351002	C3	H	2200p	350V	5%	250332200
R4	V	11k	¼W	1%	198141104	C4	P	0.5-5p	2kV		290060060
R5	V	1.1k	¼W	1%	198131104	C5	P	0.5-5p	2kV		290060060
RV1	Multi-turn 20k Cermet		½W	10%	124042000						
RV2	Multi-turn 2k Cermet		½W	10%	124032000						




TO
GUARD
HI 1
RLQ1
16
15
14
1
HI 2
BOARD 2
FROM I.P SKT
(V)
13
12
11
RLQ2
LO 2
2,4
10
9
8
RLQ3
7
6
5
RLQ4
LO 1
FROM
AC CONV O.P
HI 5
LO 5
NOTE: RELAYS ARE SHOWN IN D.C (RELAXED) P

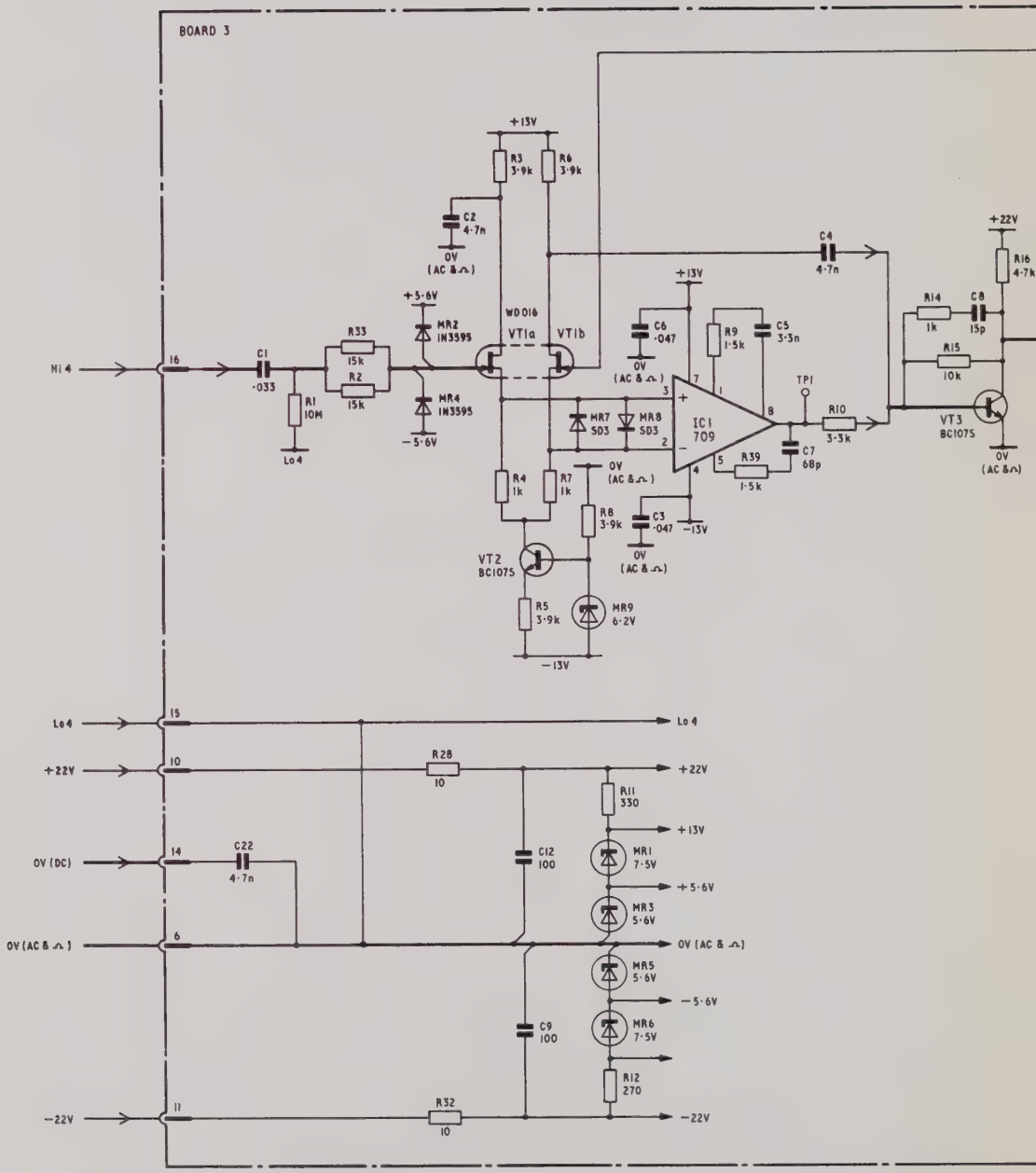


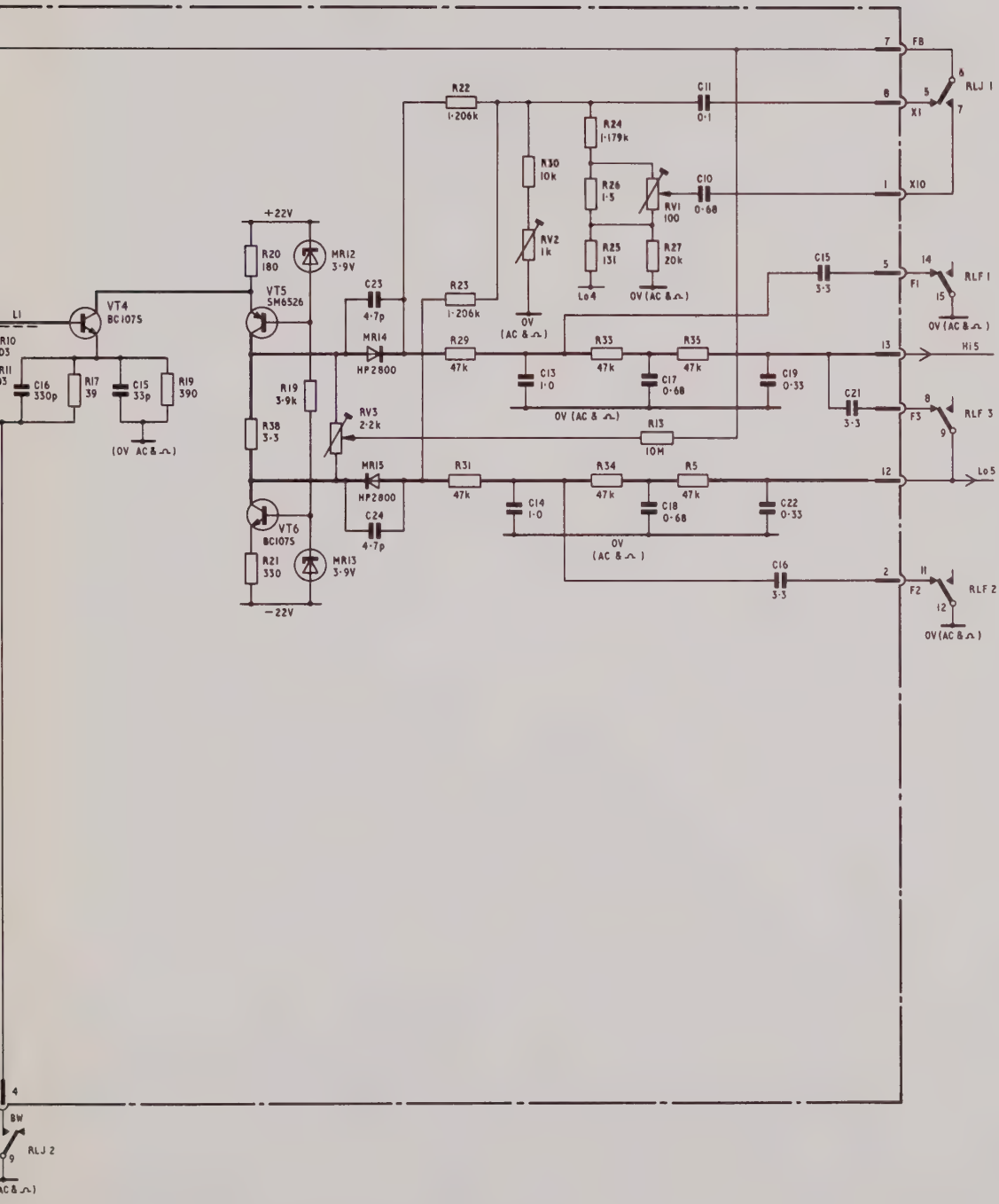
C14949302/01

AC ATTENUATOR, BOARD 2

C4
R7
R4
MR8
MR7
R6
R3
C7
R39
IC1
VT1
MR2
MR4
MR1
MR3
MR5
MR6
C2
R37
R2
C22
R8
MR9
R5
VT2
C5
R9
C6
C3
C1
I6
R1
TP1
R11
R10
C8
R14
R16
R15
C12
R12
MR10
MR11
R17
VT3
R18
R28
MR12
R20
L1
VT4
R13
MR14
C23
VT5
R19
MR13
R38
RV3
C9
VT6
R32
C24
R21
MR15
R23
R22
C11
R24
R35
R33
R29
R36
R34
R31
RV2
C20
C19
RV1
R27
R30
R25
R26
C18
C17
C10
C21
C14
C16
C13
C15

AD 1494003


BOARD 3
+13V
R3 3·9k
R6 3·9k
C2 4·7n
0V (AC & ⏦)
+5·6V
MR2 IN3595
WD016
VT1a
VT1b
R33 15k
R2 15k
MR4 IN3595
-5·6V
Hi 4
16
C1 ·033
R1 10M
Lo4
C4 4·7n
+22V
R16 4·7k
R14 1k
C8 15p
R15 10k
VT3 BC107S
0V (AC & ⏦)
C6 ·047
0V (AC & ⏦)
R9 1·5k
C5 3·3n
TP1
IC1 709
MR7 SD3
MR8 SD3
R10 3·3k
C7 68p
R39 1·5k
R4 1k
R7 1k
0V (AC & ⏦)
R8 3·9k
C3 ·047
-13V
VT2 BC107S
R5 3·9k
MR9 6·2V
-13V
Lo4
15
Lo4
+22V
10
R28 10
+22V
R11 330
+13V
0V (DC)
14
C22 4·7n
C12 100
MR1 7·5V
+5·6V
MR3 5·6V
0V (AC & ⏦)
6
0V (AC & ⏦)
MR5 5·6V
-5·6V
C9 100
MR6 7·5V
R12 270
-22V
11
R32 10
-22V

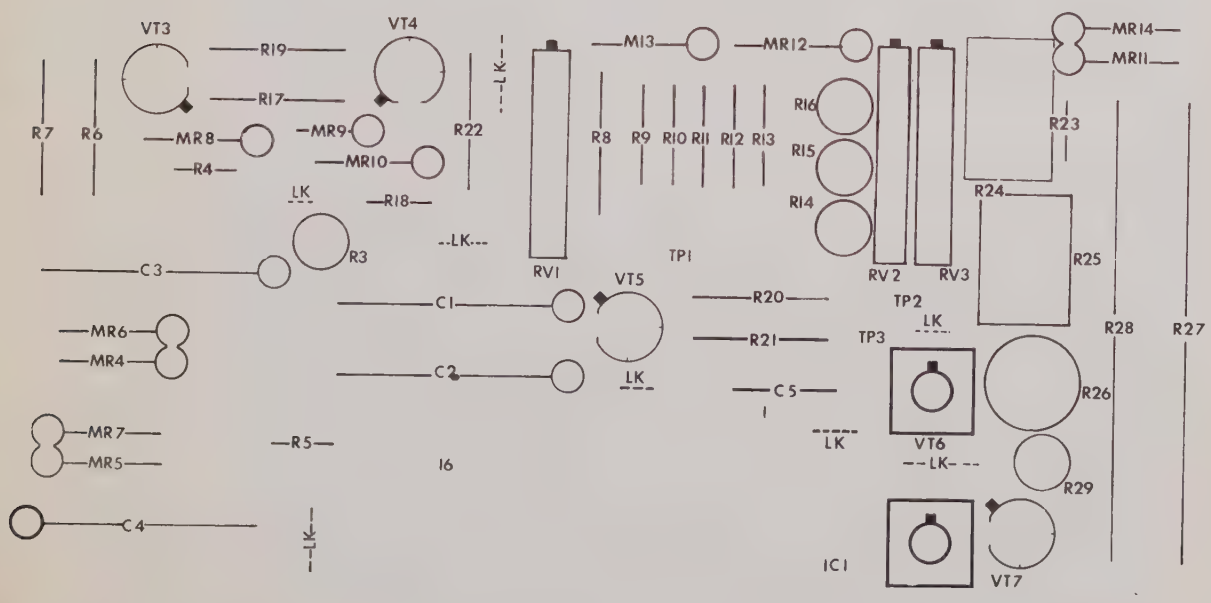


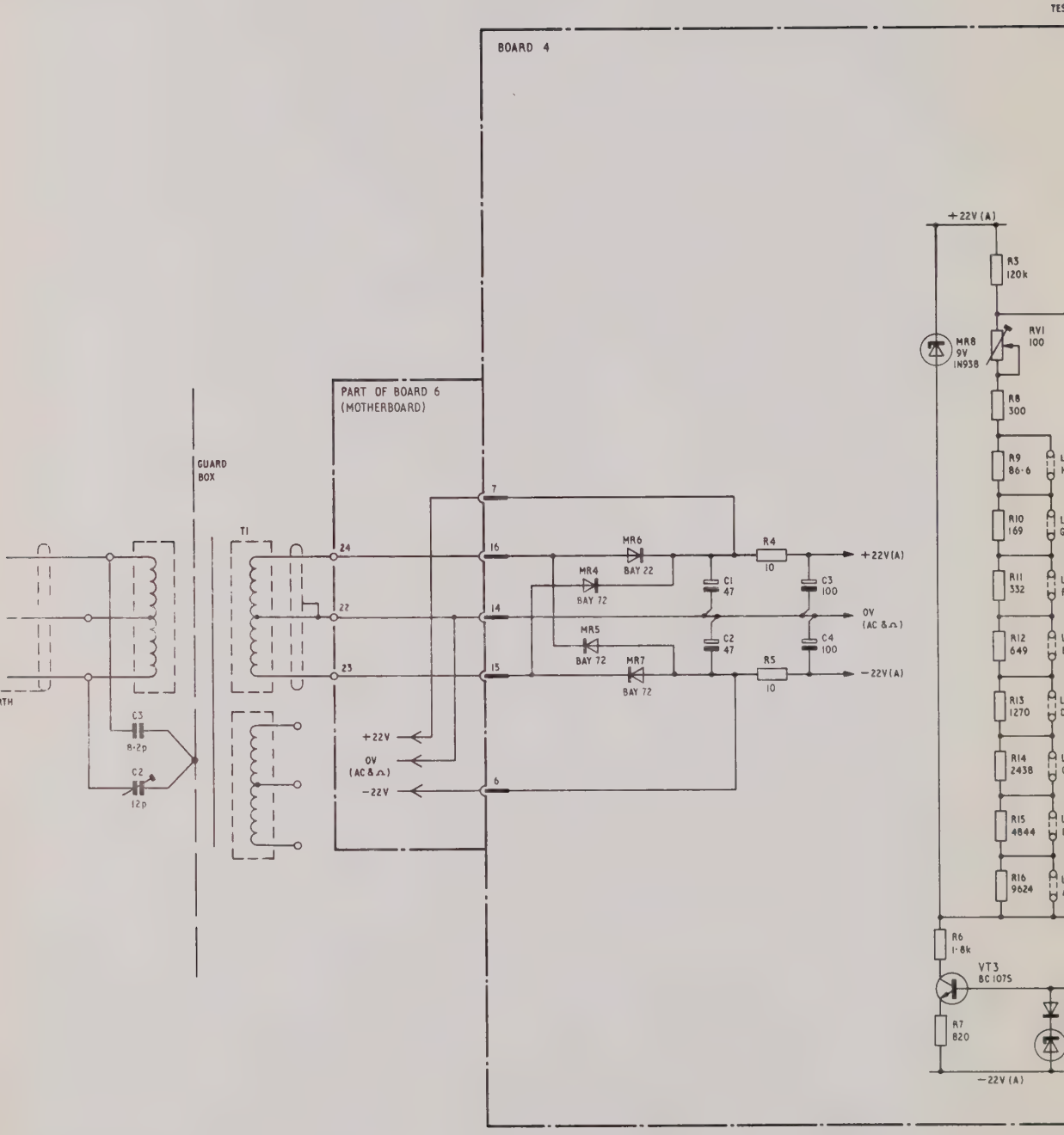
D14949303/01

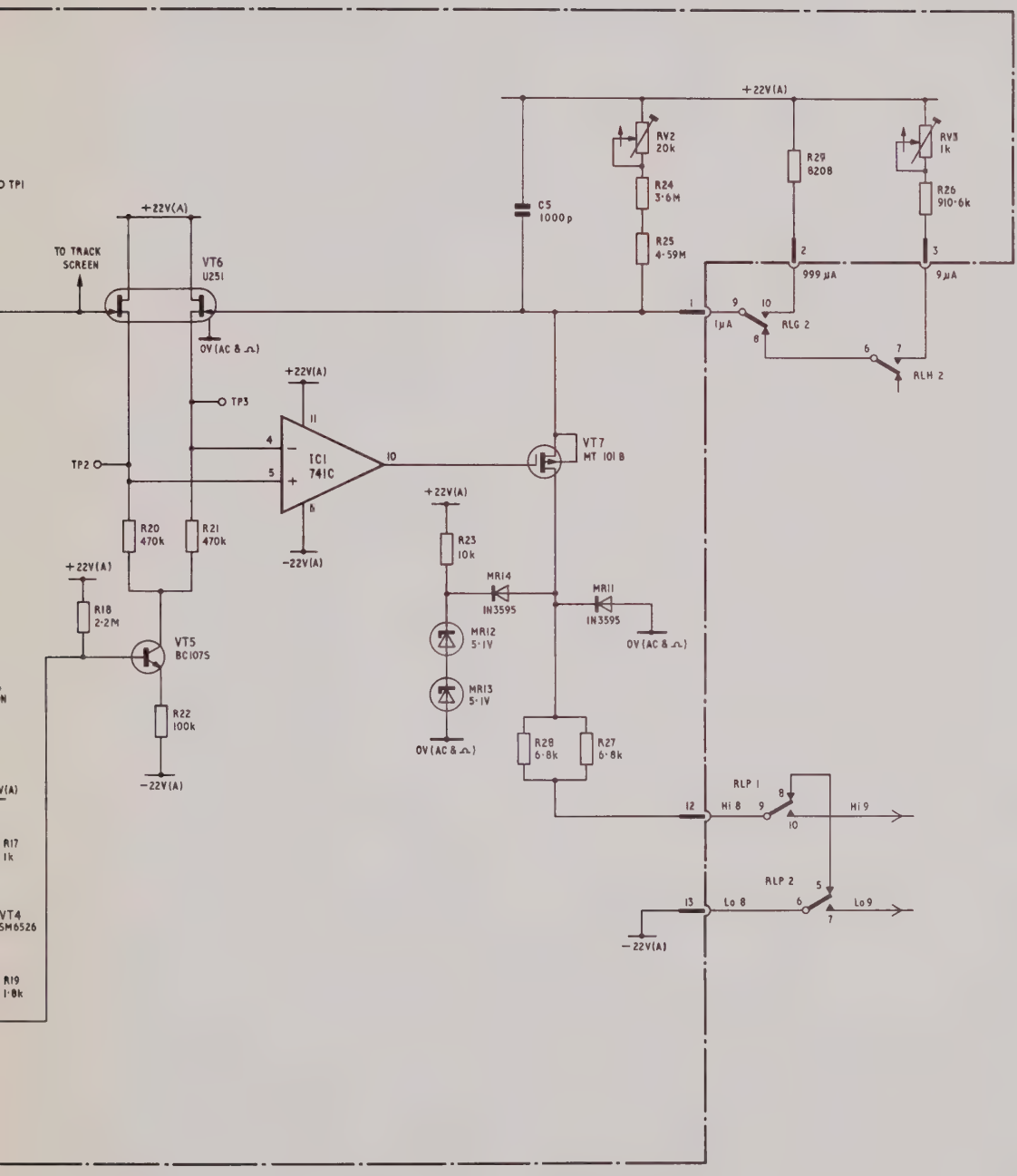
AC CONVERTER, BOARD 3

OHMS UNIT, BOARD 4

Cct. Ref.		General Description			Solartron Part No.
R3	Y	120k		0.1%	169603501
R4	X	10	1/8W	10%	172011000
R5	X	10	1/8W	10%	172011000
R6	Z	1.8k	¼W	1%	198331802
R7	Z	820	¼W	1%	198328202
R8	Z	300	¼W	1%	198323004
R9	Z	86.6	¼W	1%	160400417
R10	Z	169	¼W	1%	160400418
R11	Z	332	¼W	1%	160400419
R12	Z	649	¼W	1%	160400420
R13	Z	1270	¼W	1%	160400430
R14	Y	2438	¼W	0.1%	169603101
R15	Y	4844	¼W	0.1%	169603001
R16	Y	9624	¼W	0.1%	169602901
R17	Z	1k	¼W	1%	198331002
R18	X	2.2M	1/8W	10%	172072200
R19	Z	1.8k	¼W	1%	198331802
R20	Z	470k	¼W	1%	198354702
R21	Z	470k	¼W	1%	198354702
R22	Z	100k	¼W	1%	198351002
R23	X	10k	¼W	1%	172041000
R24		3.6M	Matched set of		169603601
R25		4.59M	Precision Resistors		
R26	Y	910.6k		0.005%	169603301
R27	Y	6.8k	6W	5%	174336800
R28	Y	6.8k	6W	5%	174336800
R29	Y	8208	¼W	0.005%	169603403
RV1	Multi-turn Wire-wound	100			122021000
RV2	Multi-turn Wire-wound	20k			122042000
RV3	Multi-turn Wire-wound	1k			122031000
C1	L	47	35V	±20%	266074700
C2	L	47	35V	±20%	266074700
C3	J	100	25V	+80% -20%	270781000
C4	J	100	25V	+80% -20%	270781000
C5	B	1000p	400V	10%	222331000
IC1	741C				510000591
VT3	BC107S				300553320
VT4	SM6526				300552990
VT5	BC107S				300553320
VT6	Dual fet U251				300554230
VT7	Mos fet MT101B				300554220
MR4	BAY72				300524530
MR5	BAY72				300524530
MR6	BAY72				300524530
MR7	BAY72				300524530
MR8	IN938 9V Zener Diode				300524290
MR9	SD3				300522160
MR10	IN823 6V Zener Diode				300521270
MR11	IN3595				300523590
MR12	5.1V Zener Diode				300521310
MR13	5.1V Zener Diode				300521310
MR14	IN3595				300523590
	16 Way Plug				352316070




BOARD 4
PART OF BOARD 6
(MOTHERBOARD)
GUARD
BOX
T1
24
22
23
7
16
14
15
6
MR6
BAY 22
MR4
BAY 72
MR5
BAY 72
MR7
BAY 72
R4
10
R5
10
C1
47
C2
47
C3
100
C4
100
+22V(A)
0V
(AC &Ω)
−22V(A)
+22V
0V
(AC&Ω)
−22V
C3
8·2p
C2
12p
+22V(A)
R3
120k
MR8
9V
1N938
RV1
100
R8
300
R9
86·6
R10
169
R11
332
R12
649
R13
1270
R14
2438
R15
4844
R16
9624
R6
1·8k
VT3
BC107S
R7
820
−22V(A)



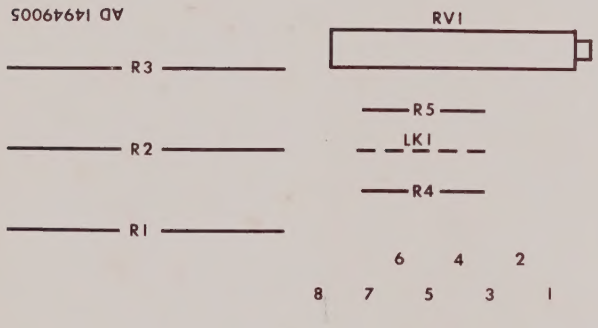
D14949304/01

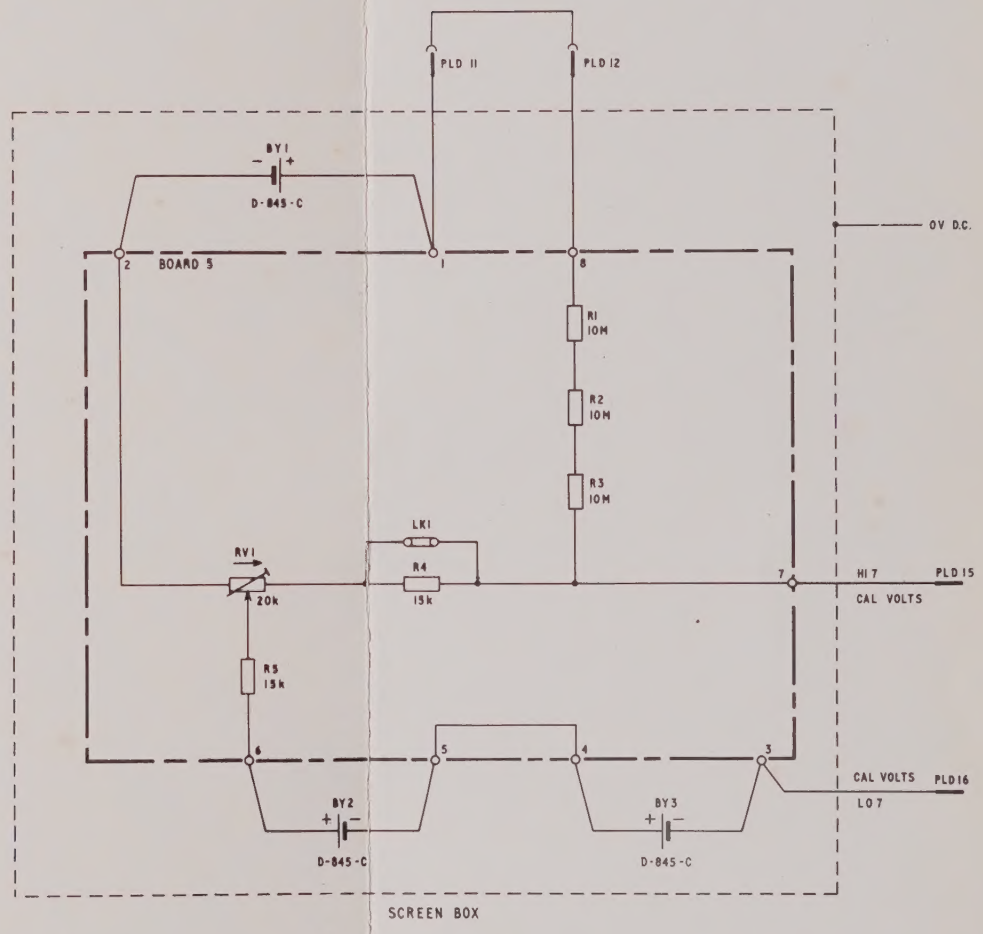
OHMS UNIT, BOARD 4

CALIBRATOR, BOARD 5

Cct. Ref.		General Description			Solartron Part No.
R1	V	10M	1W	1%	198971002
R2	V	10M	1W	1%	198971002
R3	V	10M	1W	1%	198971002
R4	V	15k	¼W	1%	198341502
R5	V	15k	¼W	1%	198341502

Cct. Ref.	General Description			Solartron Part No.
RV1	Multi-turn Wire-wound 20k	1W	5%	122042000
BY1	Standard Cell Muirhead D-845-C			310010090
BY2	Standard Cell Muirhead D-845-C			310010090
BY3	Standard Cell Muirhead D-845-C			310010090





C14949305/01 CALIBRATOR, BOARD 5

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